The Belle Silicon Vertex Detector

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6 Dec. 2008

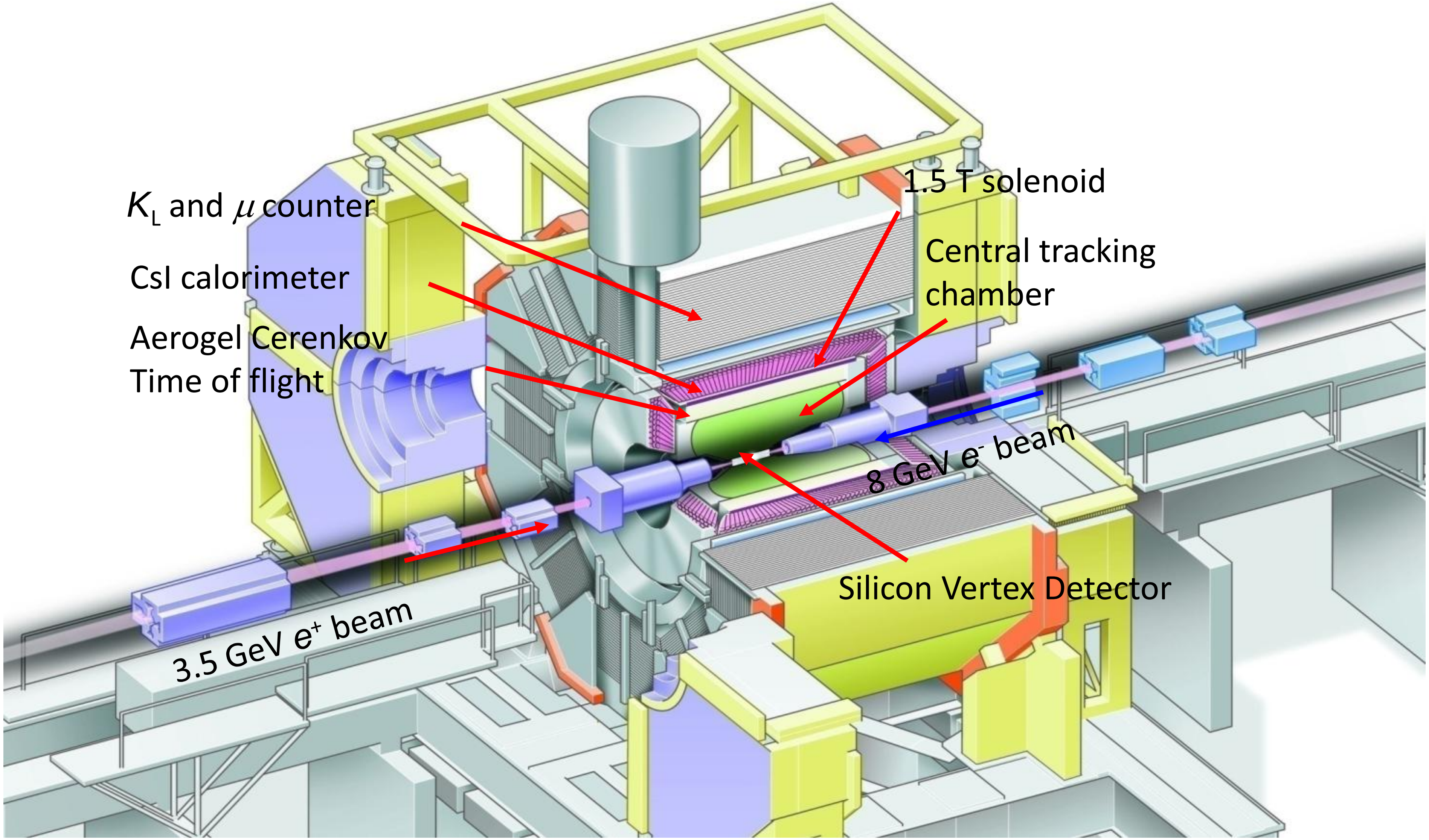
Workshop New Hadrons with Various Flavors

6-7 Dec. 2008 Nagoya Univ.

Outline

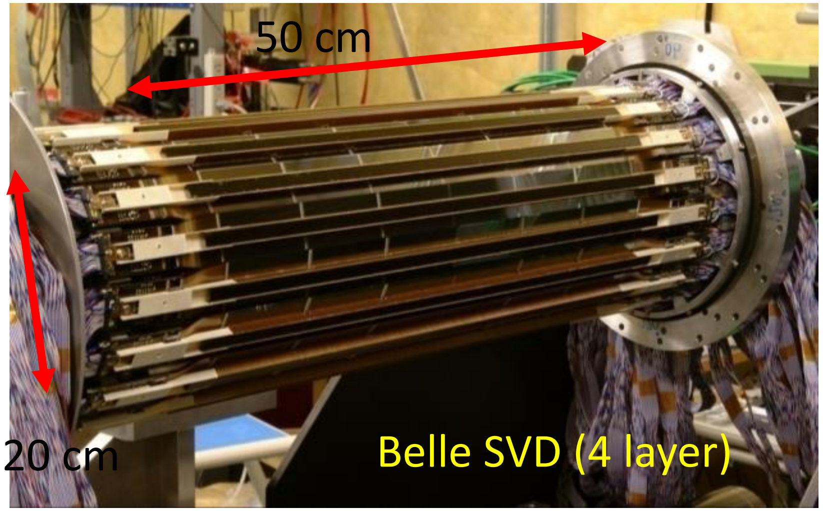
- Belle Silicon vertex detector
- Upgrade plan
- R&D and beam tests
- Synergy
- Summary

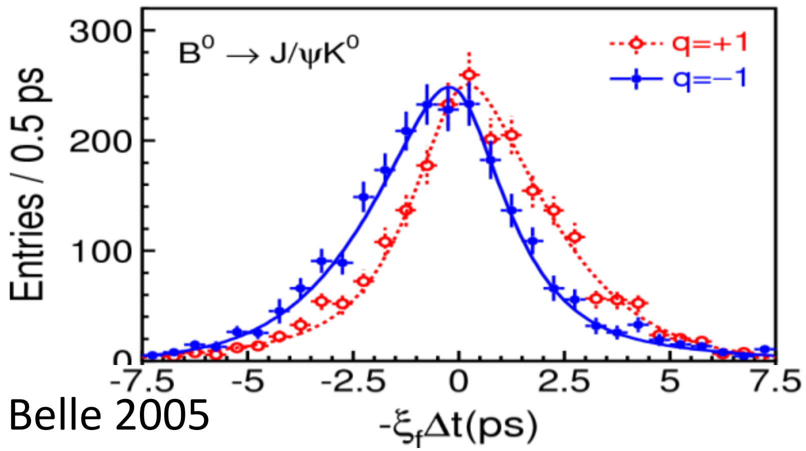
Upgrade plan of Belle silicon vertex detector



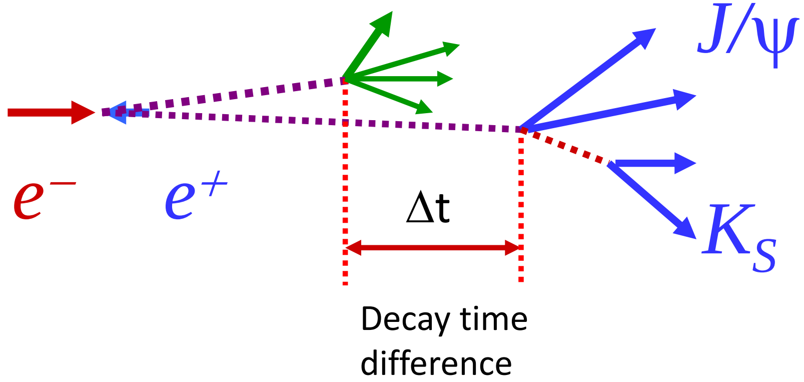
Silicon Vertex Detector

- SVD reconstructs two vertices of B decay from Υ(4S).
  - B flight length ~ 200 μm.
- The *CP* violation parameters are extracted from the distribution of distance between two vertices.





Belle 2005

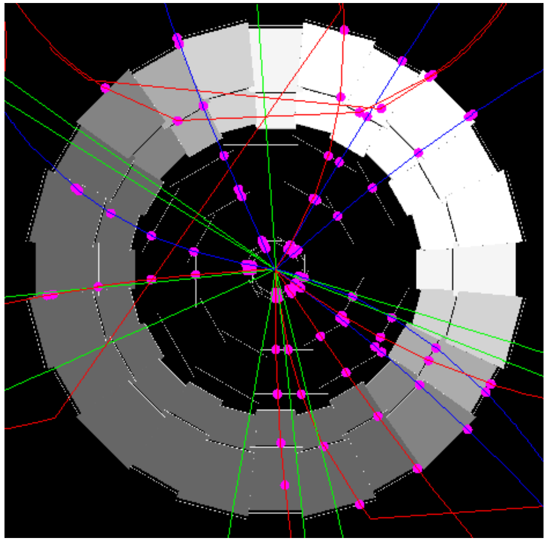


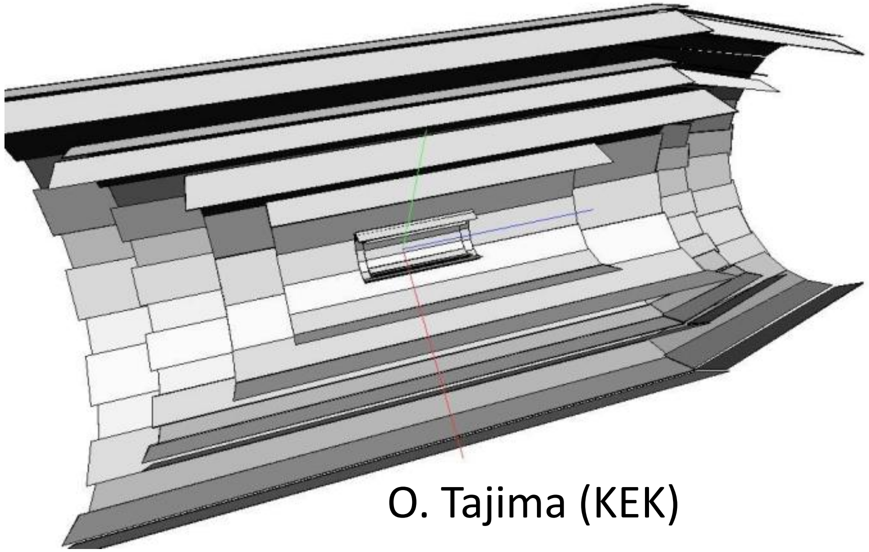
Requirements

- From view point of physics performance
  1. Low material: minimize multiple Coulomb scattering
  2. At least 4 layers: self tracking of low-pt tracks.
  3. Detector acceptance
  4. Larger acceptance of Ks (Large radius)
- From view point of detector performance
  1. Collision interval: 2 nsec.
  2. Background reduction. (Short shaping time)
  3. Trigger rate: 30 kHz at maximum
  4. Trigger latency: 3 μsec.
- The current VA1TA readout can not satisfy 2-4. APV25 ASIC, that was developed for CMS experiment at LHC satisfies all the requirements.

Detector configuration

- Configuration
  - –Six layers: for reconstruction of low-momentum tracks.
  - –Better vertex resolution.
  - –Material inside acceptance must be minimized.
- Sensor options
  - –DSSD
  - –Pixel
- Readout electronics
  - –10KHz max. ave. trigger rate
  - –Hit occupancy should be kept <10%



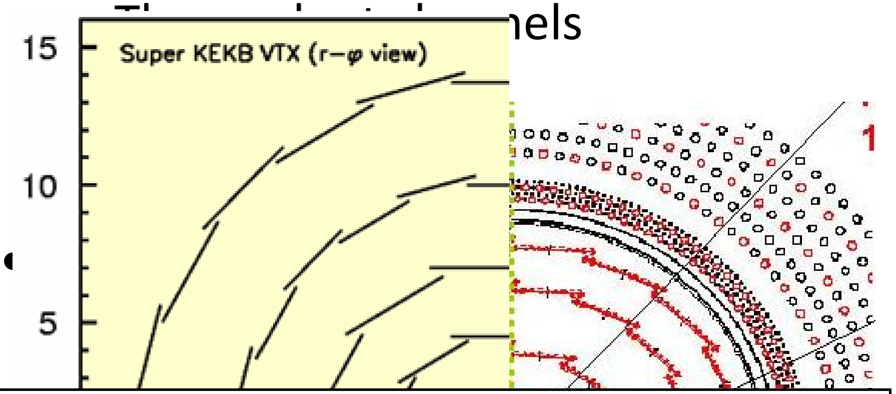


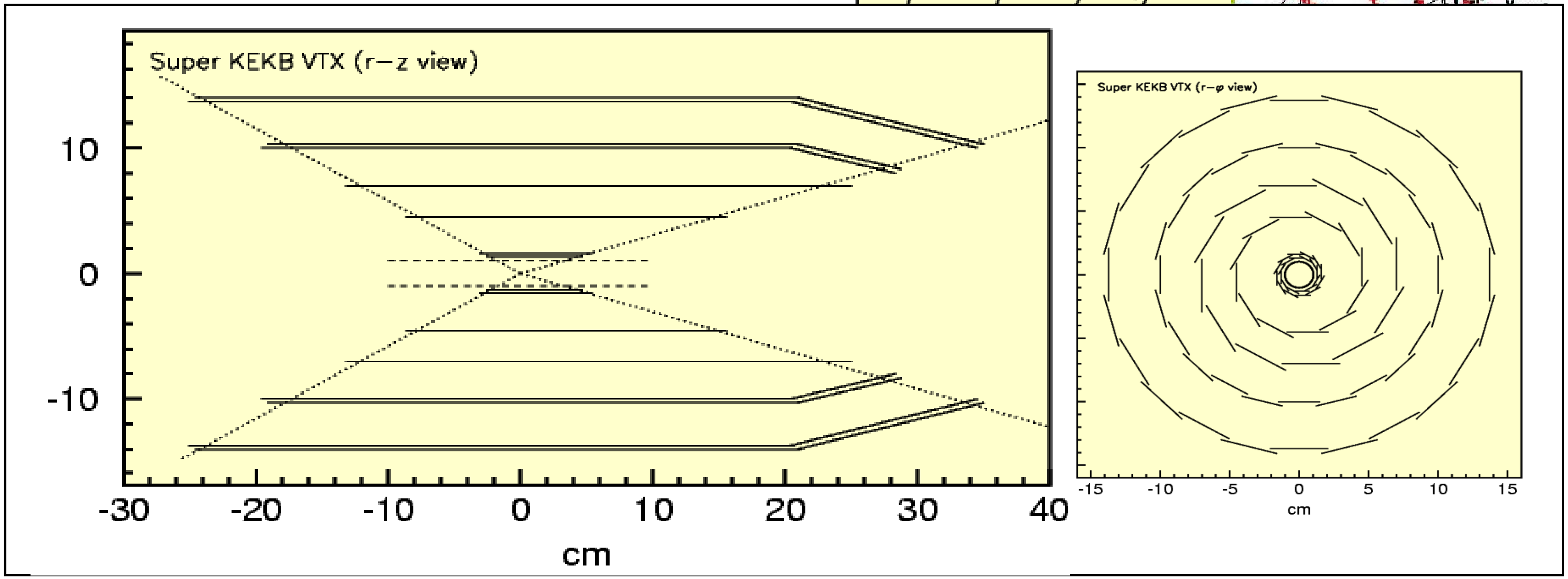
O. Tajima (KEK)

Sensor configuration

- Belle acceptance: $17<\theta<150^{o}$
- Outer radius: 150 mm
- Inner radius:13 mm
  - Beam pipe (r = 10mm)
  - For better vertex resolution.
- Total sensitive area ~ 1 m^2

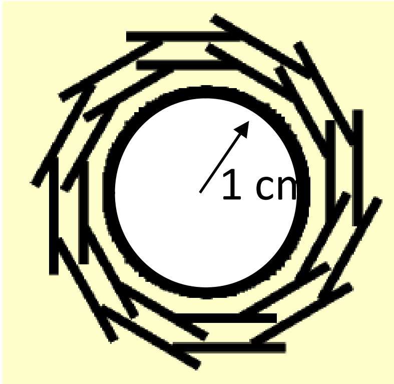
- Inclined ladders in Layer 5 and 6

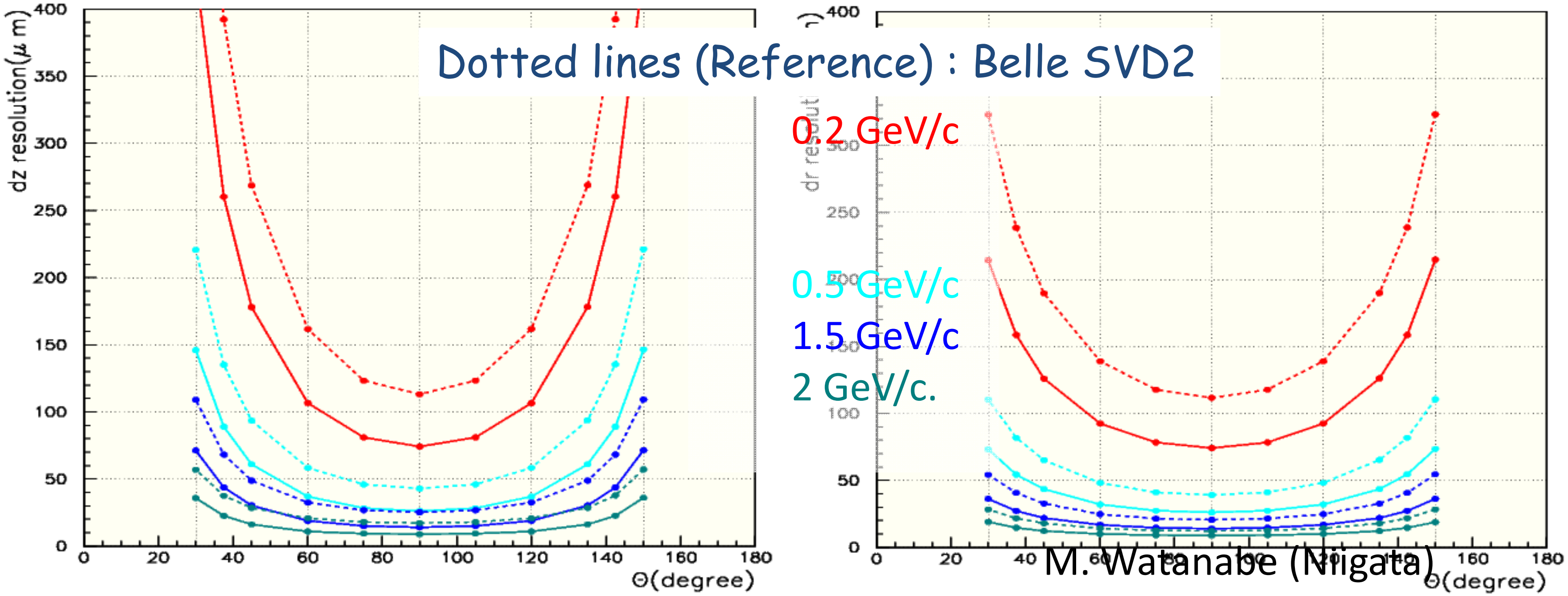




Consideration of the inner most layer (I)

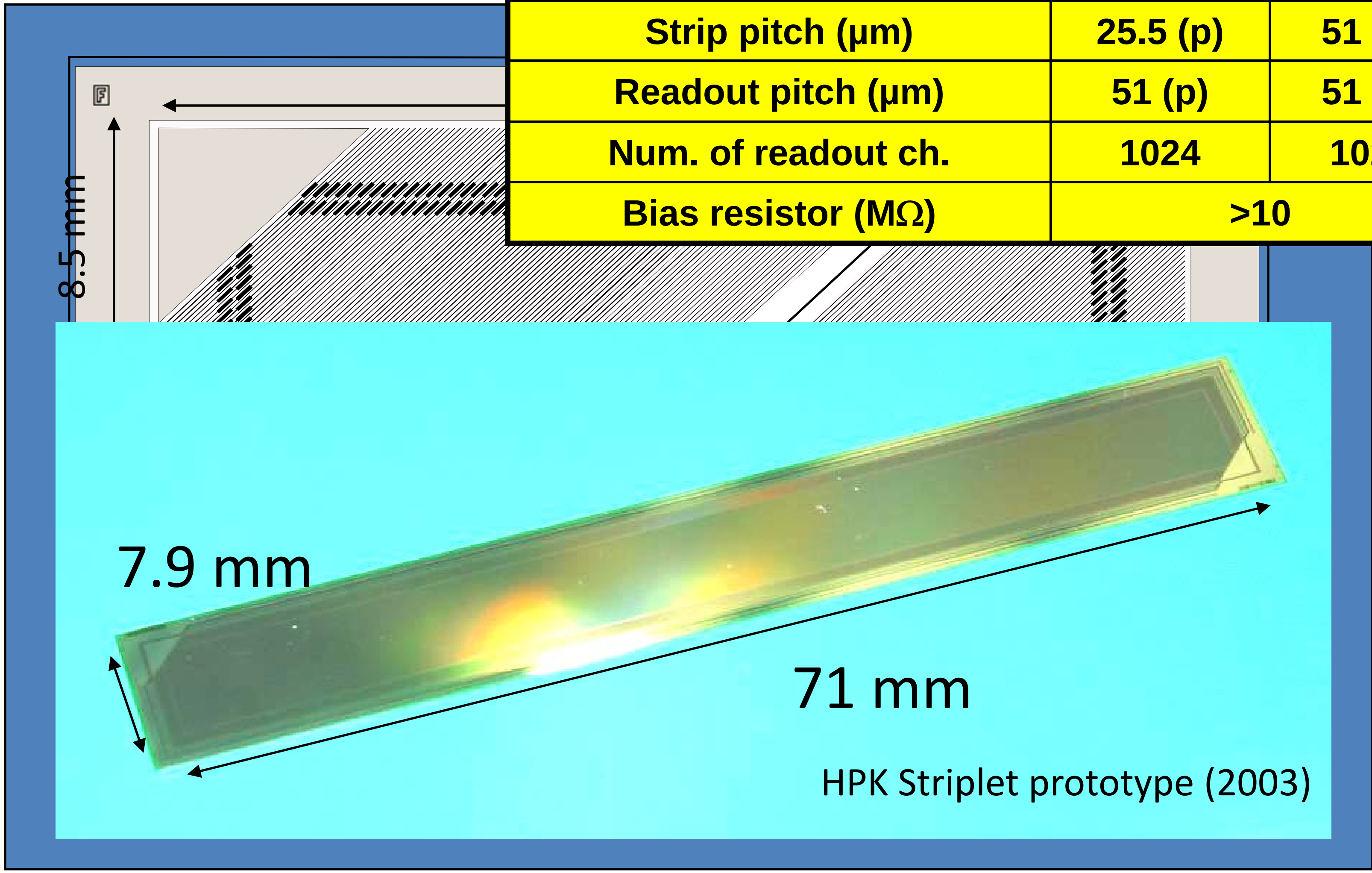
- Two layers DSSD:
  - 20 % improvement at high momentum thanks to the smaller detector radius.
  - Robust hit finding under back ground.
- Monolithic Pixel:
  - Similar performance and robust tracking
  - Recently a Germany group propose DEPFET pixel detector.





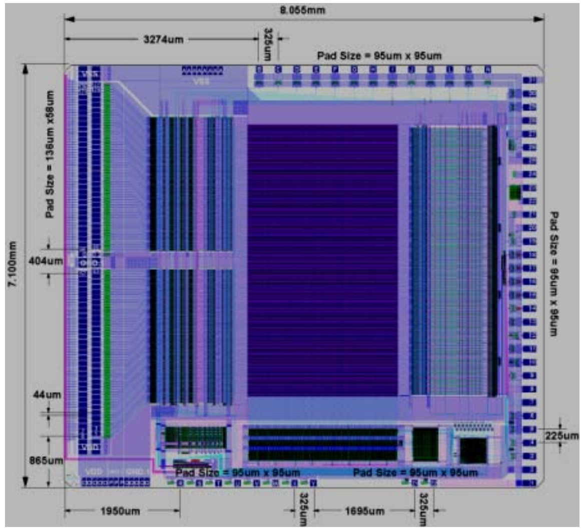
Striplet Prototyp

Parameters	p	n
Sensitive area (mm^2)	71.0x7.9	
Strip length (mm)	10.5	
Strip pitch (μm)	25.5 (p)	51 (n)
Readout pitch (μm)	51 (p)	51 (n)
Num. of readout ch.	1024	1024
Bias resistor (MΩ)	>10	

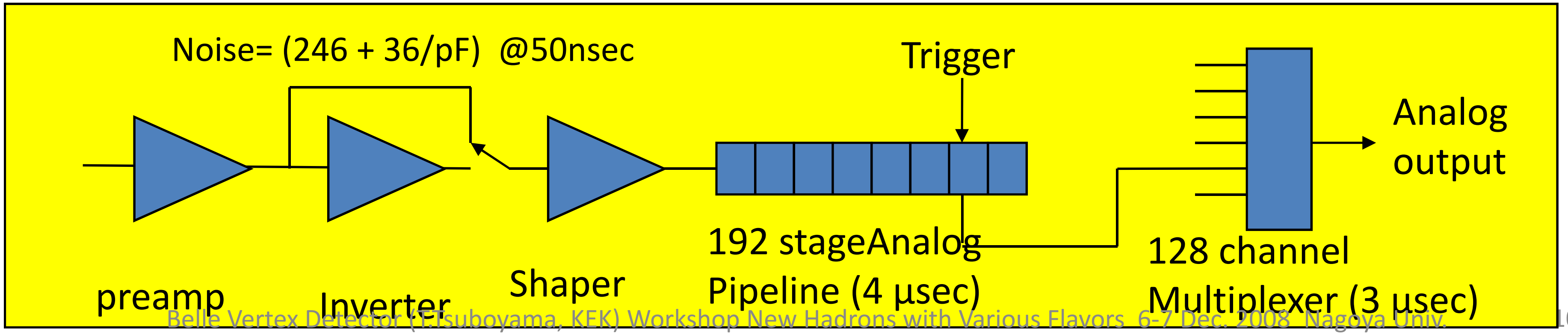


HPK Striplet prototype (2003)

Readout with APV25 ASIC

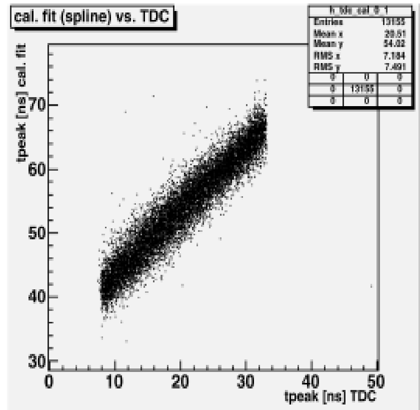


- APV25:
  - –192 stage pipeline (~4 μsec trigger latency)
  - –Up to 32 readout queues
  - –128 ch analog multiplexing (3 μsec@40 MHz)
  - –Dead time: negligible at expected trigger rate of 10 kHz
- Operated with CDAQ 42MHz clock.
  - – Recently CDAQ clock of 64 MHz is proposed. (APV25 clock will be 32 MHz)



Hit timing reconstruction

- APV25 pipe line can be used as a wave form sampler.
  - Read out 3, 6 … slices in the pipeline for one trigger.
  - Extract the hit timing information from wave form.
- Proven in beam tests: Resolution ~ 2 nsec.
- Reconstruction done in the FPGA chips in FADC board.
- (Proposed by Vienna group)



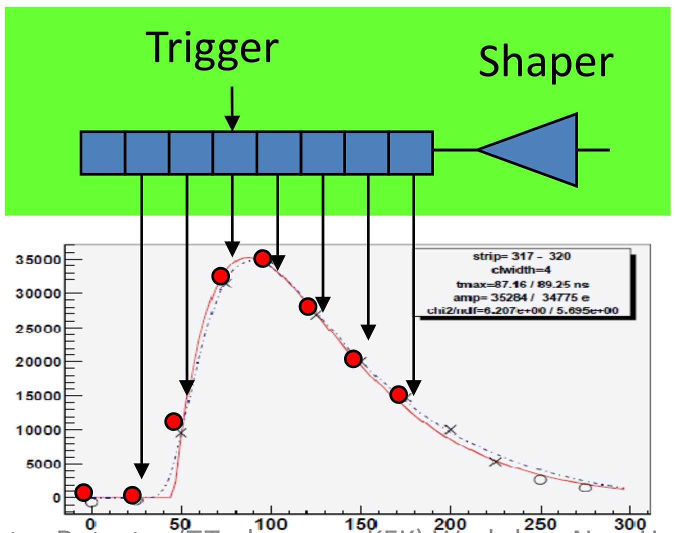
TDC vs. fitted peak time

run019, 51μm

Residual distribution (including trigger jitter)

p-side: RMS=2.16ns

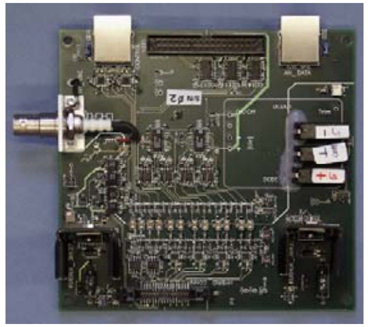
n-side: RMS=1.56ns (narrower clusters)

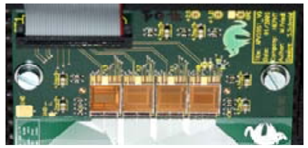


(HEPHY Vienna)

Test bench of APV25 (APVDAQ)

- Developed by HEPHY (Vienna) for adaptation test of APV25 in Belle.
  - Operated with various APV25 modes
  - External and internal trigger.
  - Evaluations: test-pulse, radiation source, IR pulse laser and test beam line.
- Hardware:
  - VME board (Control / FADC)
  - AC coupled Repeater
  - Four-chip Hybrid
- Software
  - GUI version (NI "*Lab Windows*")
  - C / Linux version (developed with Princeton group)





Beam tests

2005.04 --- Evaluation of striplet sensor readout with APV25

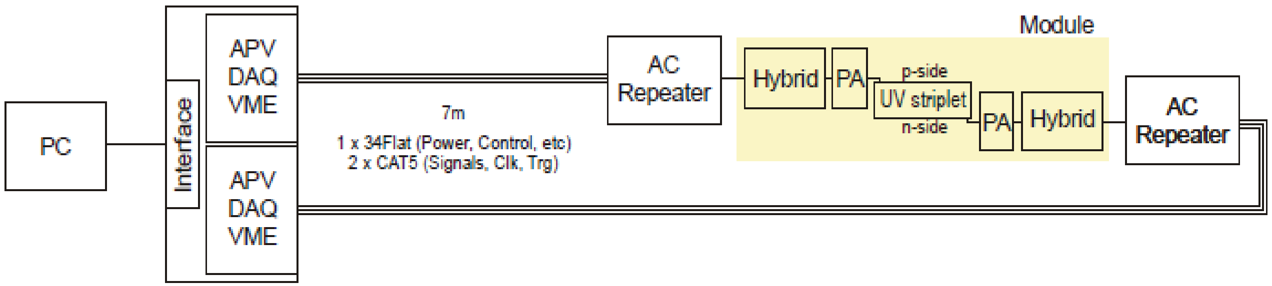
2005.12 --- Evaluation of DSSD for the SVD upgrade (APV25+VA1 readout mixed)

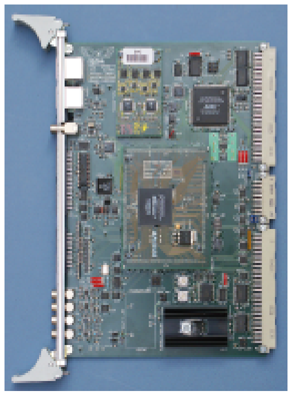
2007.11 --- Evaluation of new readout system for Belle SVD upgrade.

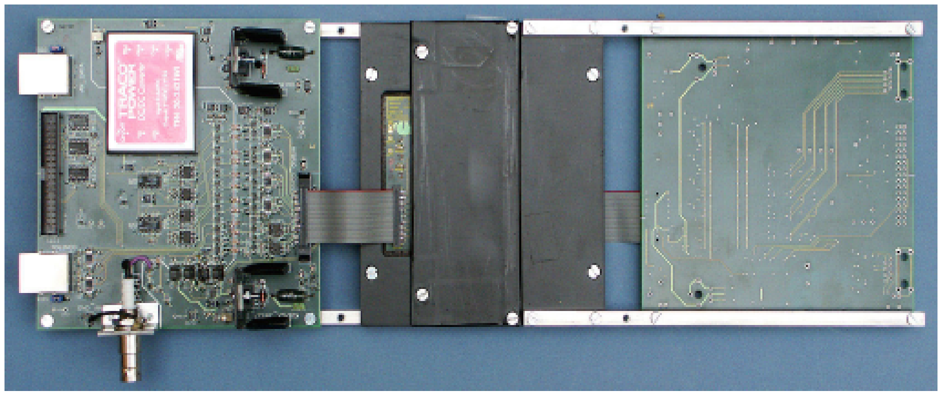
April 2005

M. Friedl | Beam Test Summary [4]/[19]

APVDAQ

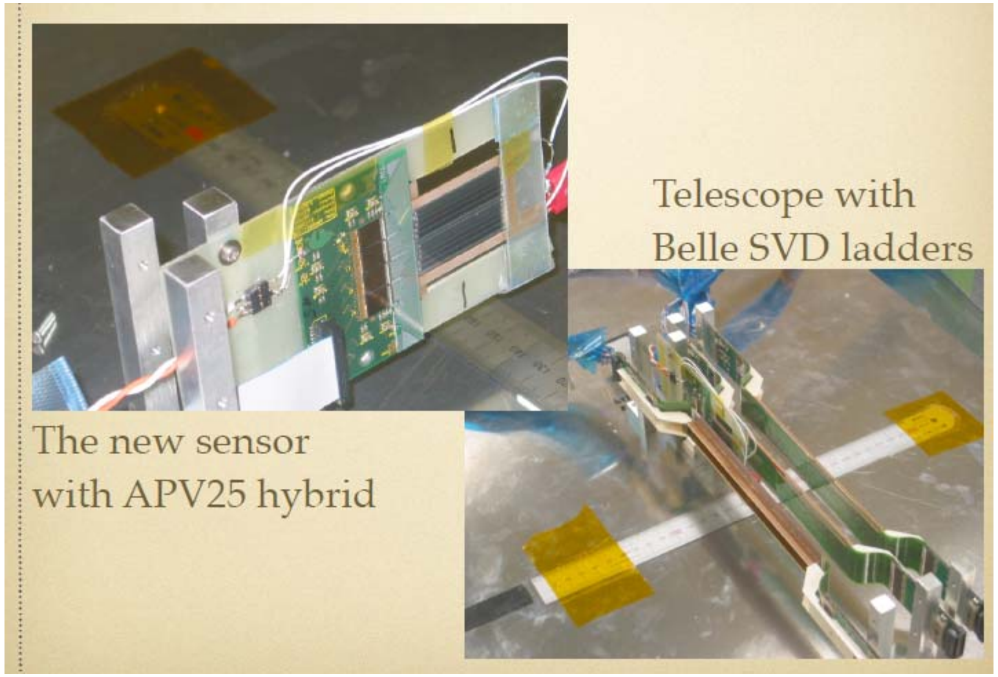


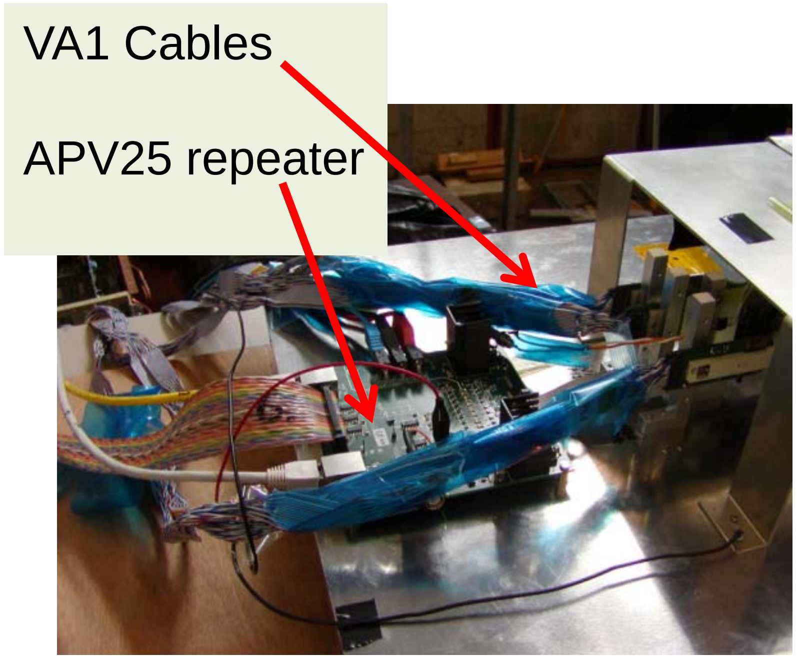




Dec. 2005

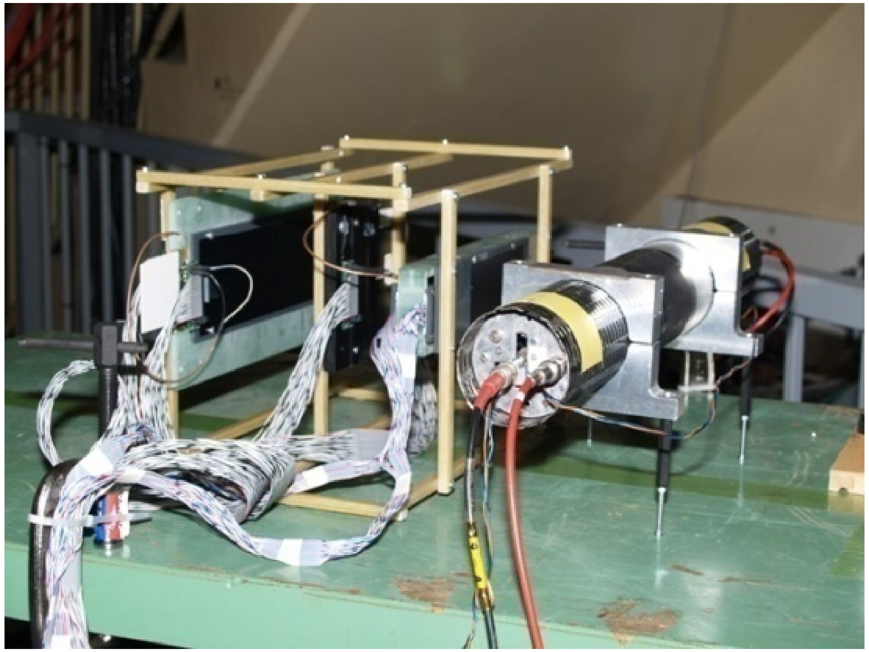
- Almost the last beam test at he KEK proton synchrotron PI-2 beam line.
- 1 APV25 and 3 VA1 ladders
- Test of the new sensor for Belle upgrade.





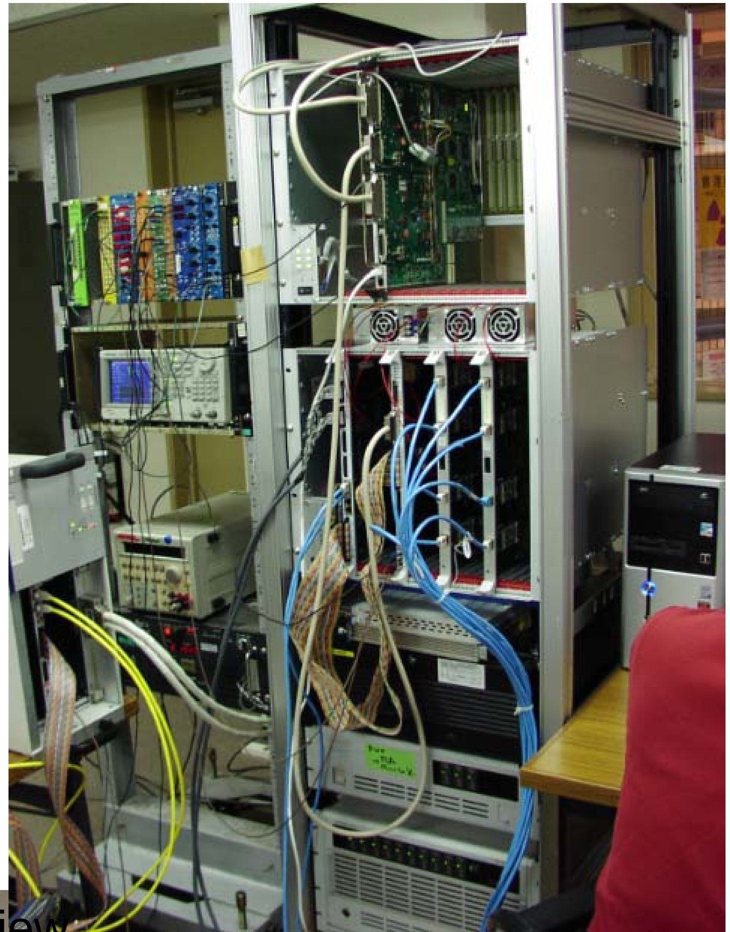
Nov. 2007

- The first experiment at the KEK Fuji beam line.
- HEPHY (Vienna), Niigata, KEK
- FADC with data sparsification FPGA code was tested.



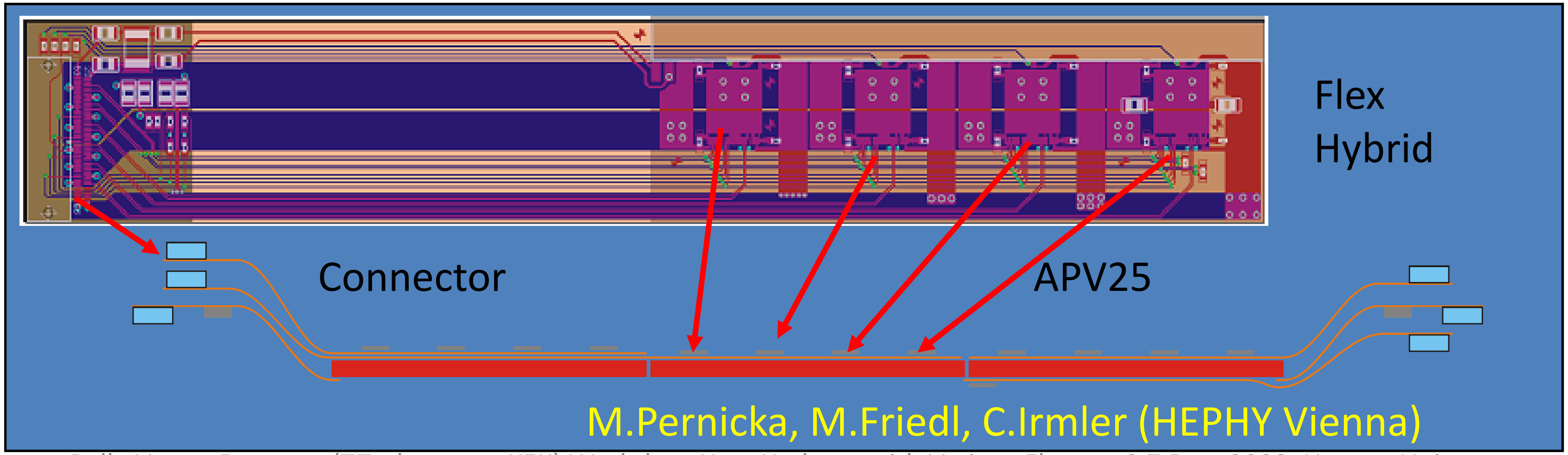
Nov 2008

- Features the test of whole readout chain:
  - APV25 → FADC → COPPER
  - Basic connection was confirmed.
  - Performance tests in progress.
- Participants: Vienna, Krakow, Kyungphook (Belle), Kyoto (Tanida group), Osaka (Hotta, Maeda).



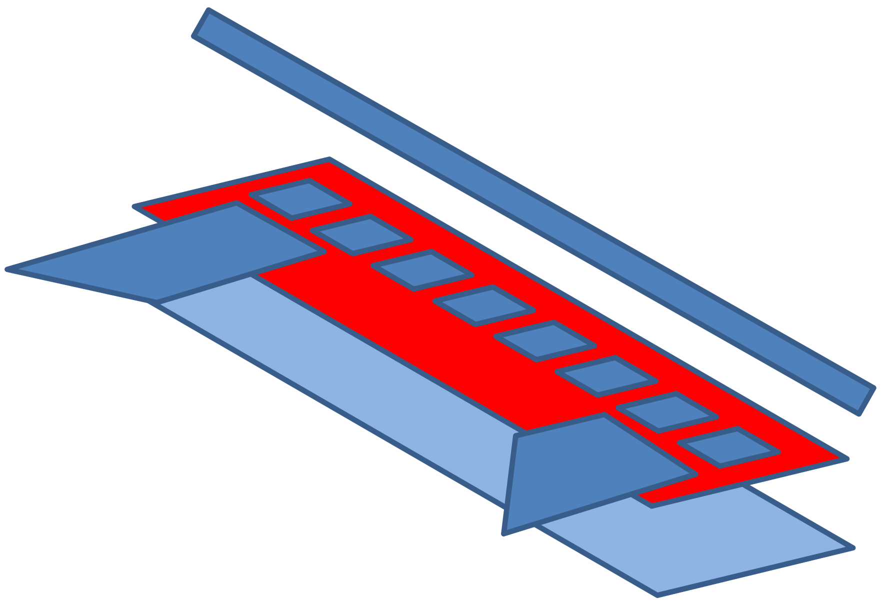
Mount readout chips on DSSDs

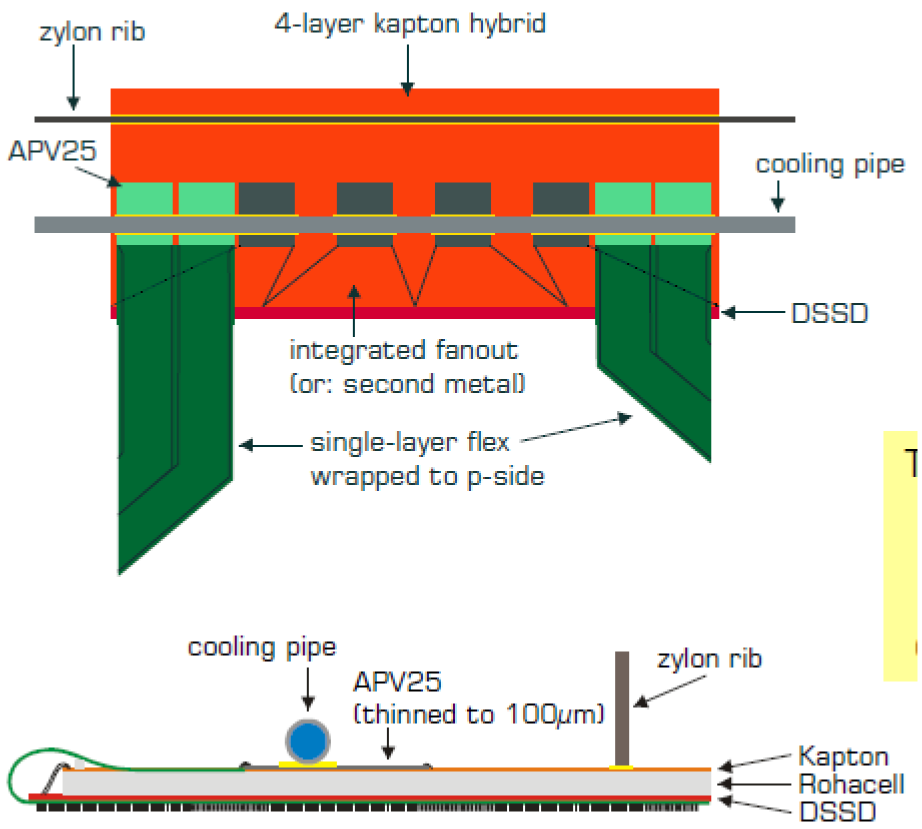
- In order to avoid the long (up to 56 cm) kapton flex, Vienna group proposed to mount the readout chips on DSSD sensors.
  - Capacitance due to long kapton flex can be avoided.
  - Detail resolution study including material budget and S/N is necessary.
  - Various cooling method will be tried. (Air, water channel …)



Origami scheme

- Using one flex hybrid and cooling tube in order to readout both sides of a DSSD.
- Benefit of APV25 on DSSD
  - No ghosts in hit reconstruction





Sensor production

- Double-sided sensor is essential to minimize the material.
- 300 μm is acceptable. The thinner the better.
- Mass production starts in 2009.
- HPK stopped the double-sided production line.
- We have started to find other suppliers.
- Korea group：Kyungpook Univ.
- Indian group: Tata Institute

Comments on the pixel detectors

- Hybrid monolithic sensor can not be used for the inner most layers.
- Monolithic Pixel detector
  - MAPS (Monolithic active pixel sensor)
  - SOI (Silicon on insulator)
  - DEPFET technology
- MAPS and SOI is made with commercial foundries.
  - Size limitation by reticle (photo mask) size.
- DEPFET pixel detector is proposed by German collaboration (May 2008).
  - Mature: Already used in various applications.
  - Can be thinned to 50 um.
  - Large area sensor can be made, not limited by reticle size.
  - Radiation tolerance is study in progress.

Software

- In Super B factory, software activities should be much more emphasized.
  - Studying rare decay modes
  - Delicate modes: Ultimate detector performance should be kept forever.
    - Calibrations.
    - Alignments of the detectors.
    - Detection performance estimation

Alignments

- Ambiguities of alignment between sensor and senor, and, between silicon vertex detector and central drift chamber are O(10 μm), in case of present Belle.
  - We guess the field non-uniformity due to final-focus magnets prevents better alignment with magnet.
- Above 5 ab^{-1} integrated luminosity (x7 of the present Belle data), statistics error of B decay vertex measurement reaches this level.
  - Physics output will be limited by sensor alignment ambiguity.
- Better detector alignment methods are necessary.

Design of the interaction region

- The Super KEKB accelerator design is extremely ambitious.
  - Huge synchrotron radiation, heat from the high current beam, and beam background is expected at the IP region.
  - It is not clear we can really escape from those effects.
- Mechanical structure as well as its radius has not been defined.
  - Radiation level can not be predicted.
  - Intense discussion is done by a Belle and KEKB joint team.
- We might start with conservative design.

Test beam facilities

- For the Belle upgrade program, I think, a good test-beam line is necessary.
  - Especially years 2009-2013 are important.
  - Pixel detctor evaluation
  - Fuji beam line stops when KEKB stops.
  - J-Parc: Far away.
  - LEPS beam line

Summary

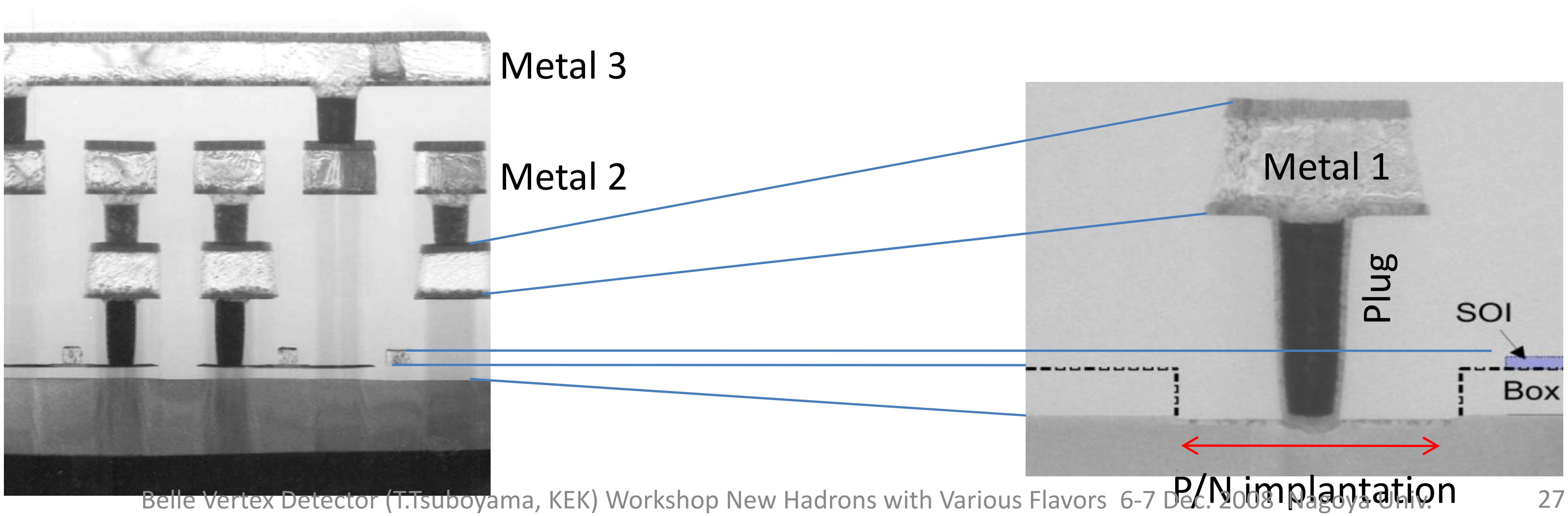
- Silicon vertex detector will be based on APV25 ASIC.
- DEPFET pixel detector will be installed.
  - Lifetime: not yet clear
- IR region scheme should be decided in roder for us to start the vertex detector design.

Progress of the SOIPIX project

- OKI 200 nm SOI CMOS process.
- Normal CMOS process.
- 2005/2006 process at the OKI experimental line (150 nm process)
- 2007 process at the OKI mass production line (200 nm process)
- 2008 Submission in preparation (Jan 2009)
- Team leader: Y.Arai yasuo.arai@kek.jp

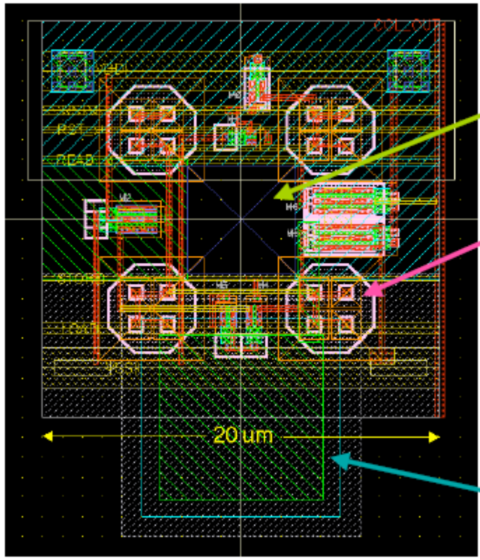
OKI SOI structure

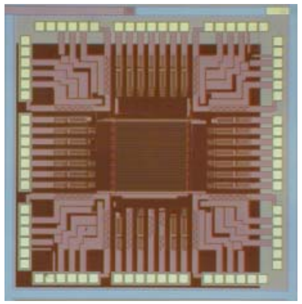
- Add a few steps to the normal CMOS production.
  - Remove the buried oxide (BOX) where implant is done.
  - Implant the P/N type ions.
  - Fill the hole with SiO2 and annealing.
  - Make a via for the contact to metal 1.
  - Fill the via with plug metal.
- Normal CMOS process will be continued.



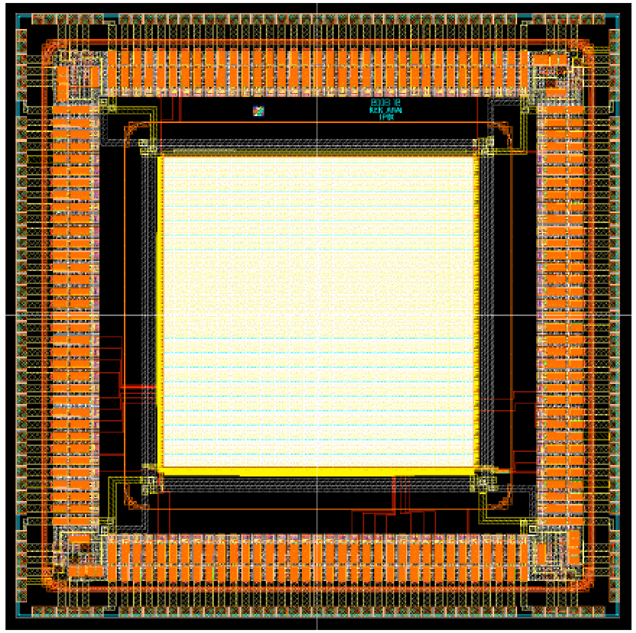
Progress of the SOIPIX project

- 2005 First submission (150 nm)
- 2006 Second submission (150 nm)
- 2007 Third submission in preparation(200 nm)





2005
2.5mmx2.5mm
32x32 cells chip



2006
5mmx5mm
128x128 cells chip

Function of the vertex detector in B factories (I)

- Basic design of Belle/Babar silicon vertex detectors is valid in Super B factories.
  - Even at 100 times larger luminosity, B factories are forever low-energy machines.
- Measure the decay vertices of the two B mesons, especially in the Z direction.
  - At Y(4S) energy, the events are either a pure BB system or non-B events.
  - If a B decay mode is identified, the other tracks and energy clusters belong to the other B.
  - Thanks to the long lifetime and slow B^0-B^0bar oscillation, the resolution of the silicon vertex detector is adequate.

Function of the vertex detector in B factories (II)

- Help the tracking by the central drift chamber
  - Extend the lever arm of high-pt tracks for B→Kπ, $\pi\pi$ etc.
  - The detection of slow π in B → D*X → DπsX.
- Ks reconstruction in B→K(*) γ.
  - Only 2 charged tracks appears separated from B decay vertex.
  - Larger radii of outer 2 layers increase the Ks acceptance.