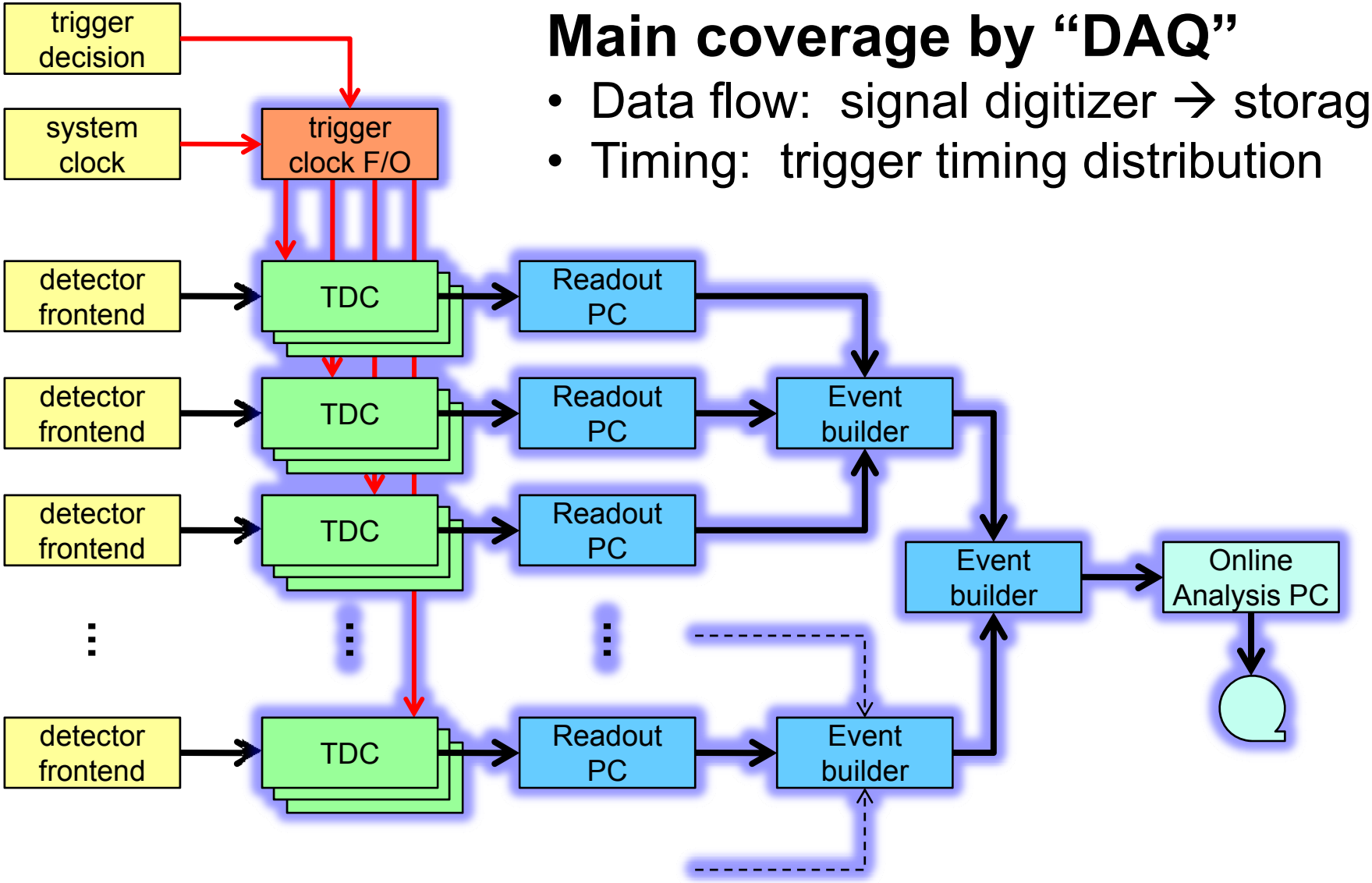
Detector R&D: Belle DAQ System

Takeo Higuchi
IPNS, KEK
Belle DAQ group

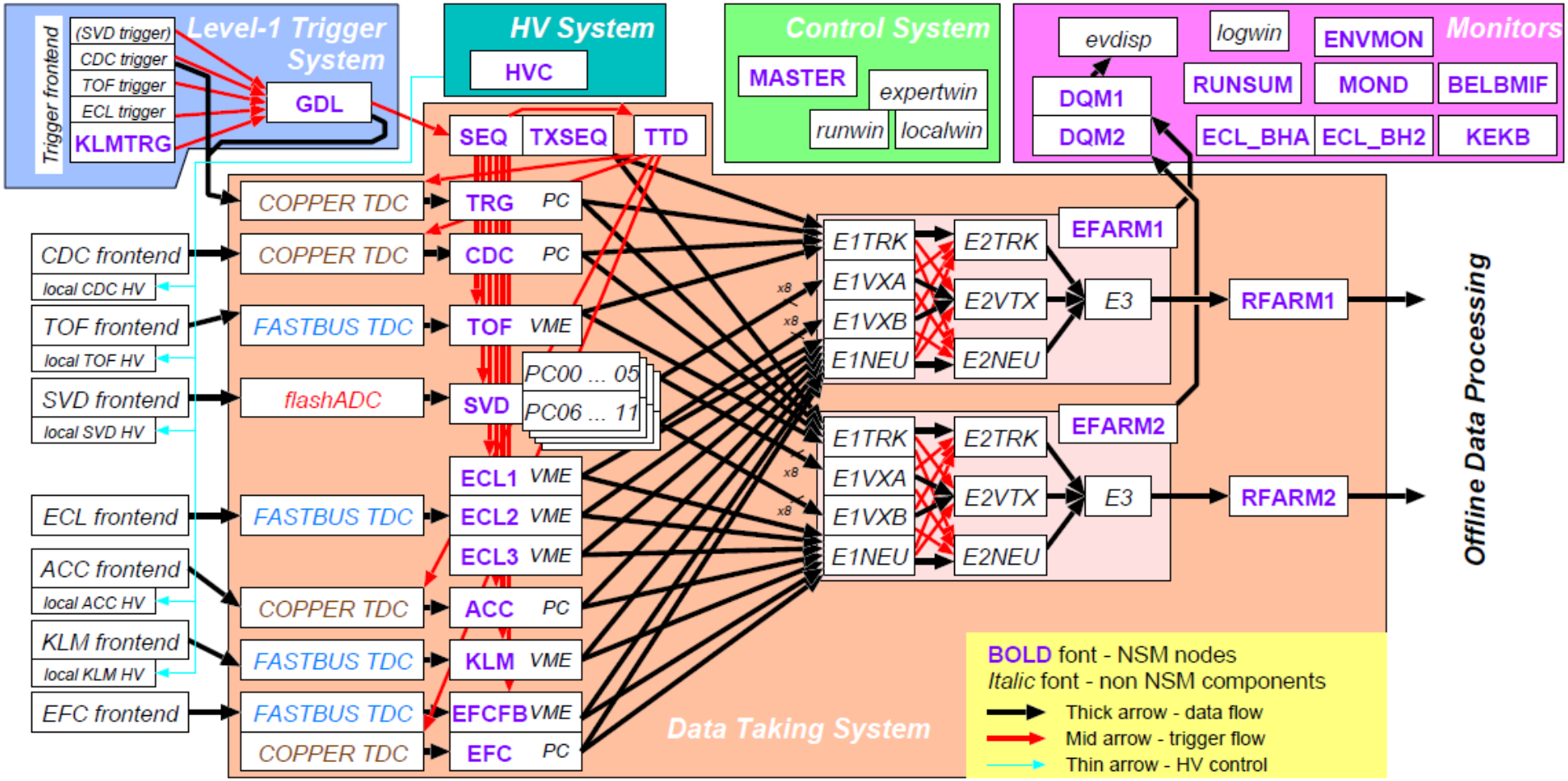
Belle DAQ Overview



Main coverage by "DAQ"

- Data flow: signal digitizer → storage
- Timing: trigger timing distribution

Belle DAQ Diagram

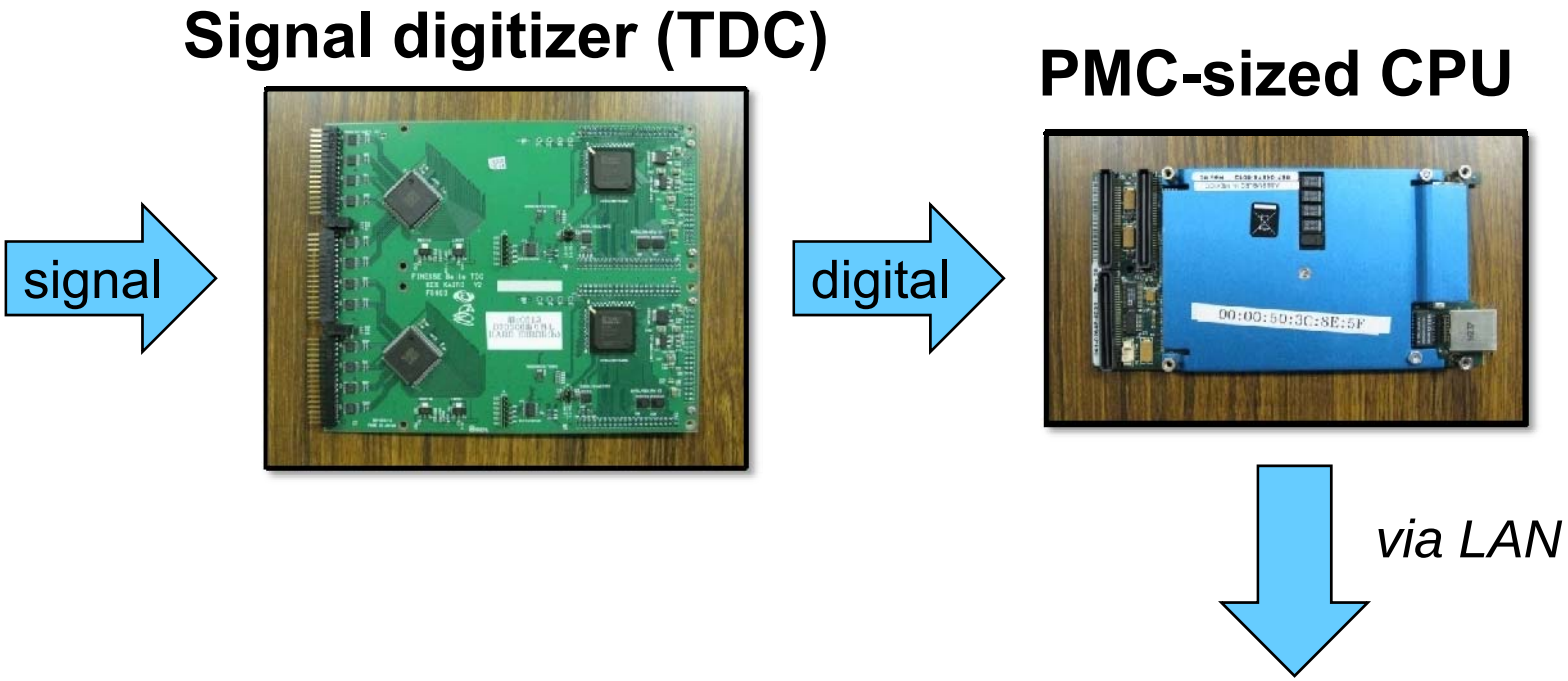


Coverage list

- **Signal digitization**
- **Digitized data readout**
- **Event building**
- **Online data analysis**
- **Timing distribution**
- Run control
- HV control
- Data quality monitor

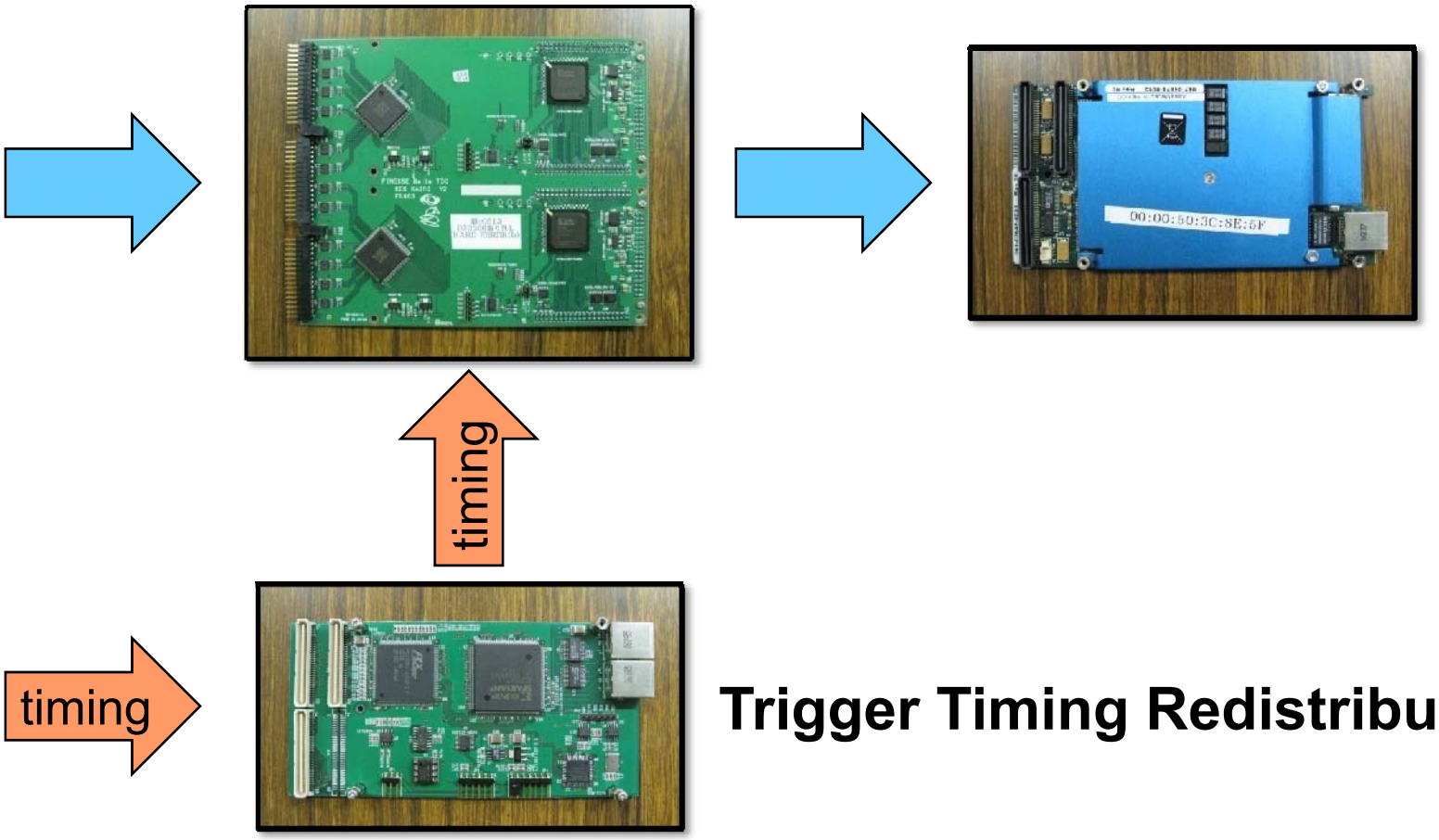
Belle DAQ Virtual Tour – 1

- **Signal digitization and data transmission**



Belle DAQ Virtual Tour – 2

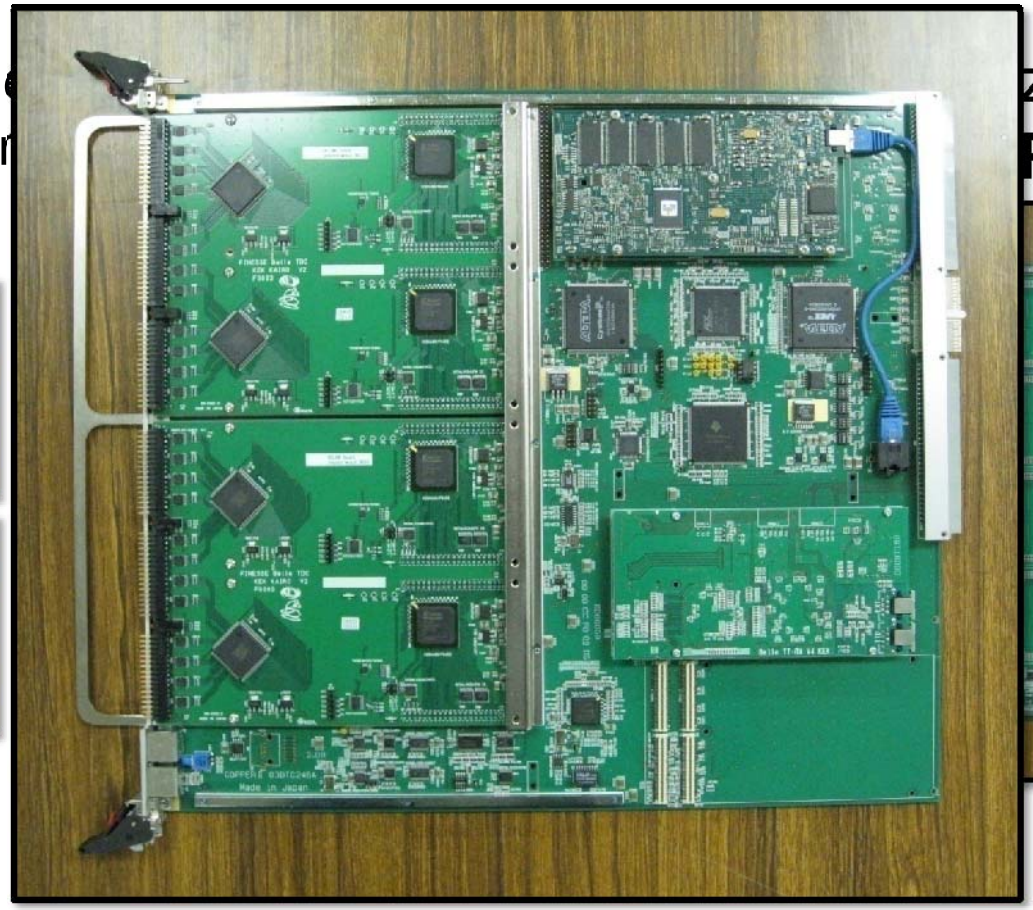
- **Trigger timing redistribution**



Trigger Timing Redistributor

Belle DAQ Virtual Tour – 3

- **COPPER**
  - TDC module
  - Trigger timing
  - PMC-sized



zed Platform

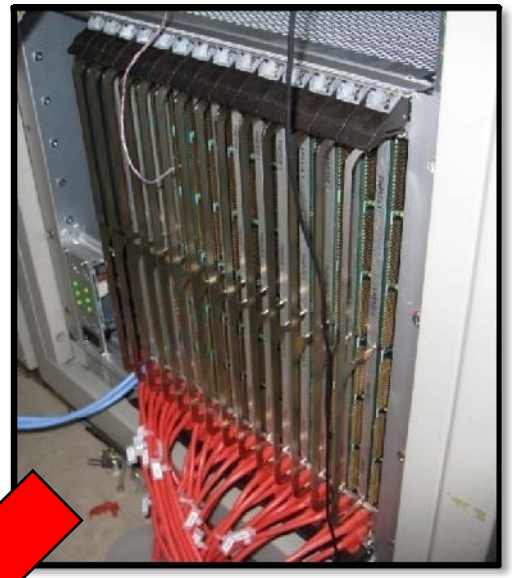
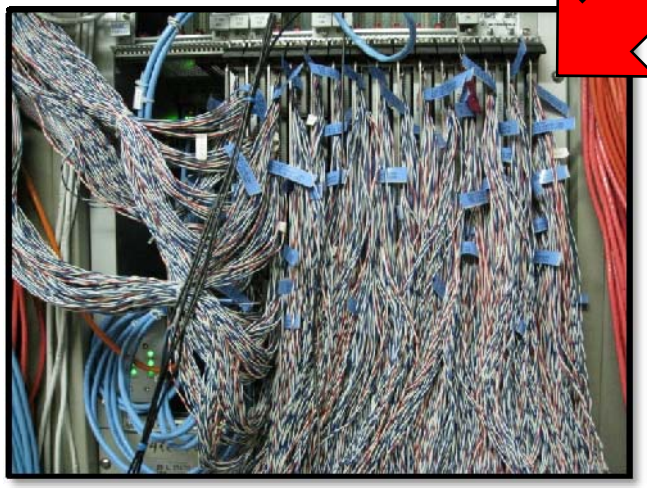
PPER”

Detail of the COPPER is described later.

Belle DAQ Virtual Tour – 4

- **COPPER crate**

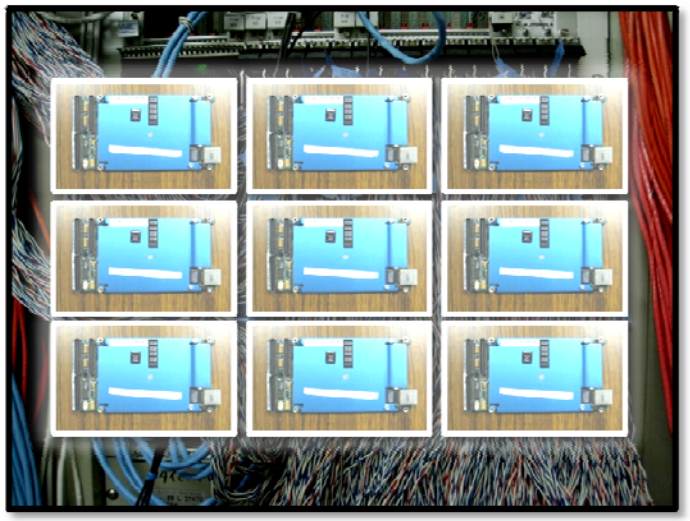


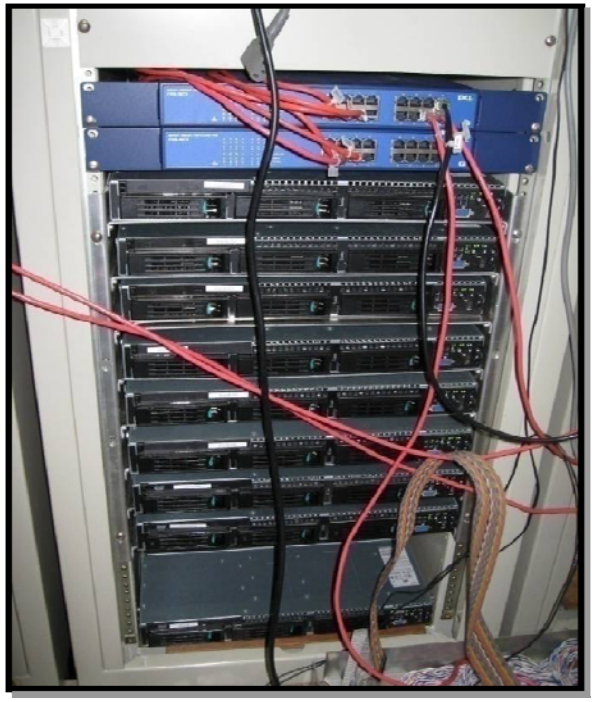
← After cabling
of input signals

Belle DAQ Virtual Tour – 5

- **Crate readout**



Digitized data readout by the PMC-sized CPU are sent to crate readout PCs via a network switch.



Belle DAQ Virtual Tour – 6

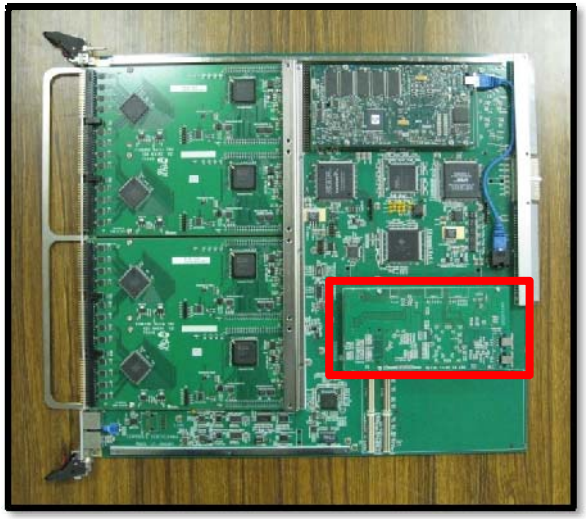
- **Event building PCs / Online analysis PCs**

Fragmented data from each crate readout PC are sent to event building PCs to be combined to a single event record.

Finally, the data are sent to online analysis PCs and recorded to hard disks.

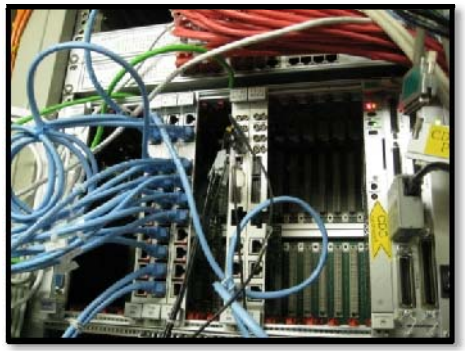
Belle DAQ Virtual Tour – 7

- **Trigger timing distribution – again**



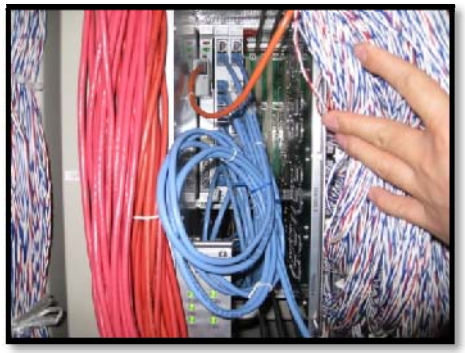
- Trigger timing distribution
- System clock distribution
- Busy collection

timing



timing

Fanout



timing

crate rear

Advertisement: COPPER System

- **We have developed several excellent DAQ technologies by ourselves.**

- **Among them, today, we like to advertise the "*COPPER System*" to you for its …**
  - High flexibility to fit your experiment,
  - Wide acceptance of L1 rate up to 30kHz,
  - Broad bandwidth of > 80MB/s,
  - Less DAQ deadtime with equipped pipeline, and
  - Less requirement of knowledge in writing readout software.

Why We Developed COPPER?

- **KEKB / Belle upgrade plan**
  - KEKB luminosity increases: **1.7×10^{34} → 8×10^{35} $cm^{-2}s^{-1}$**
    → more L1 rate: **500 Hz → 10-30 kHz**
  - Belle upgrades
    → more readout channels: **40 kB/ev → 200-300 kB/ev**

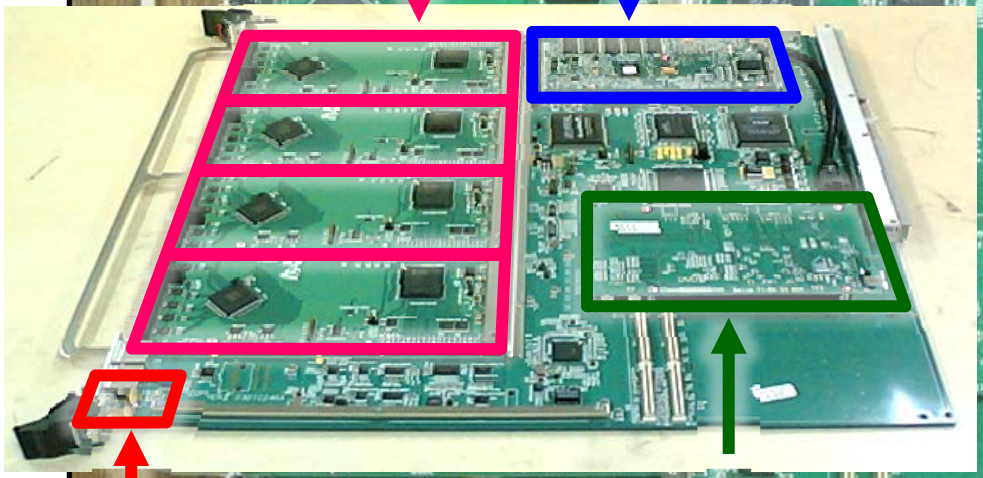
- **Limit of the present Belle DAQ**
  - Deadtime fraction of the present FASTBUS-based DAQ will be extrapolated to ~20% even @ L1=1kHz.

Call for new DAQ accommodates with L1=30kHz.

COPPER

FINESSE×4
Add-on modules to the COPPER. Responsible to digitize the input signals and output them to pipeline FIFOs on the COPPER.

Online CPU
Add-on module to the COPPER. Responsible to readout the COPPER FIFO, to process and format the data, andto send the data to external PC via the network.

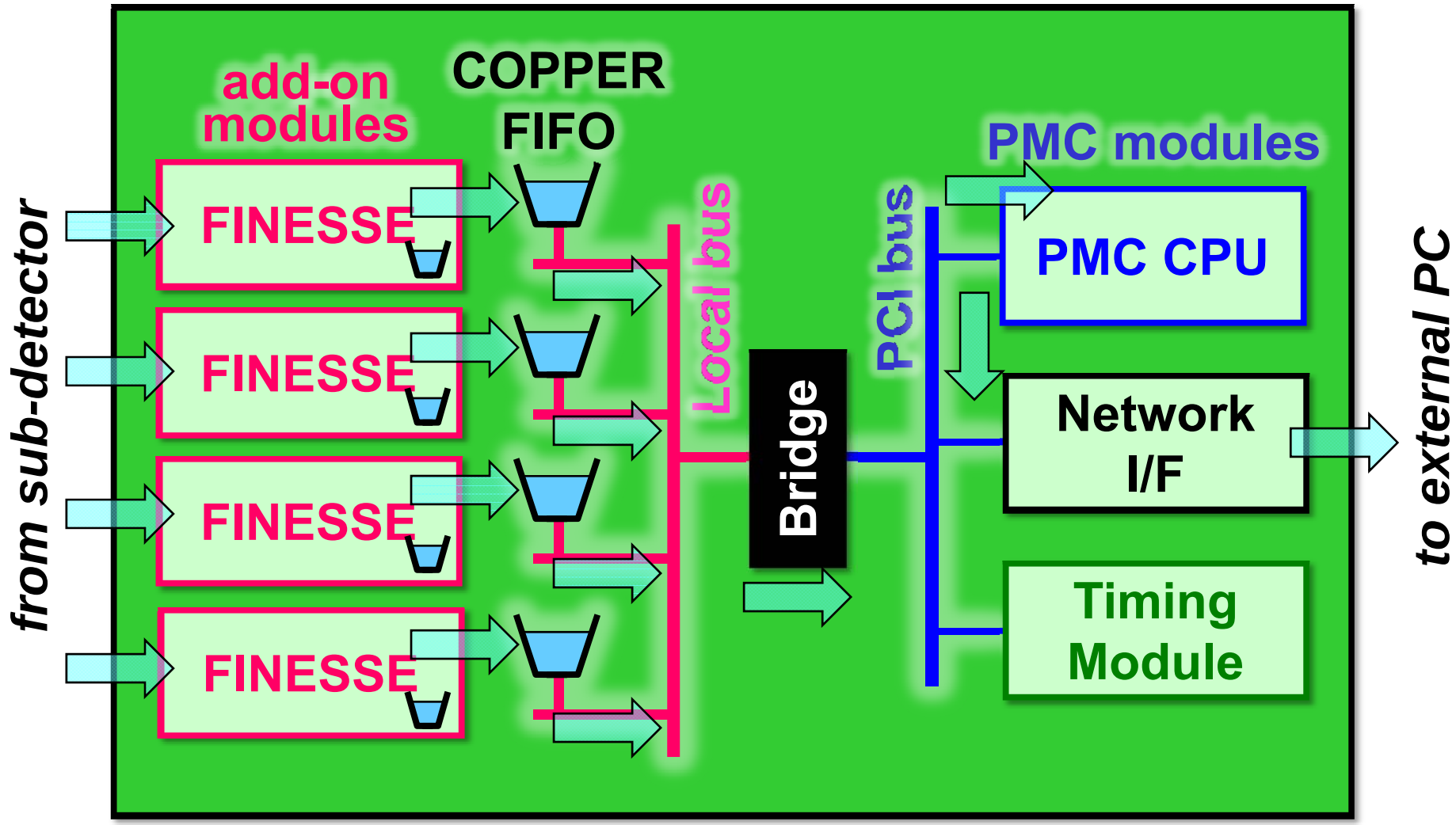


RadiSys EPC-6315
- **Intel P3 800 MHz**
- **256 MB memory**
- Network boot
- RedHat Linux 9

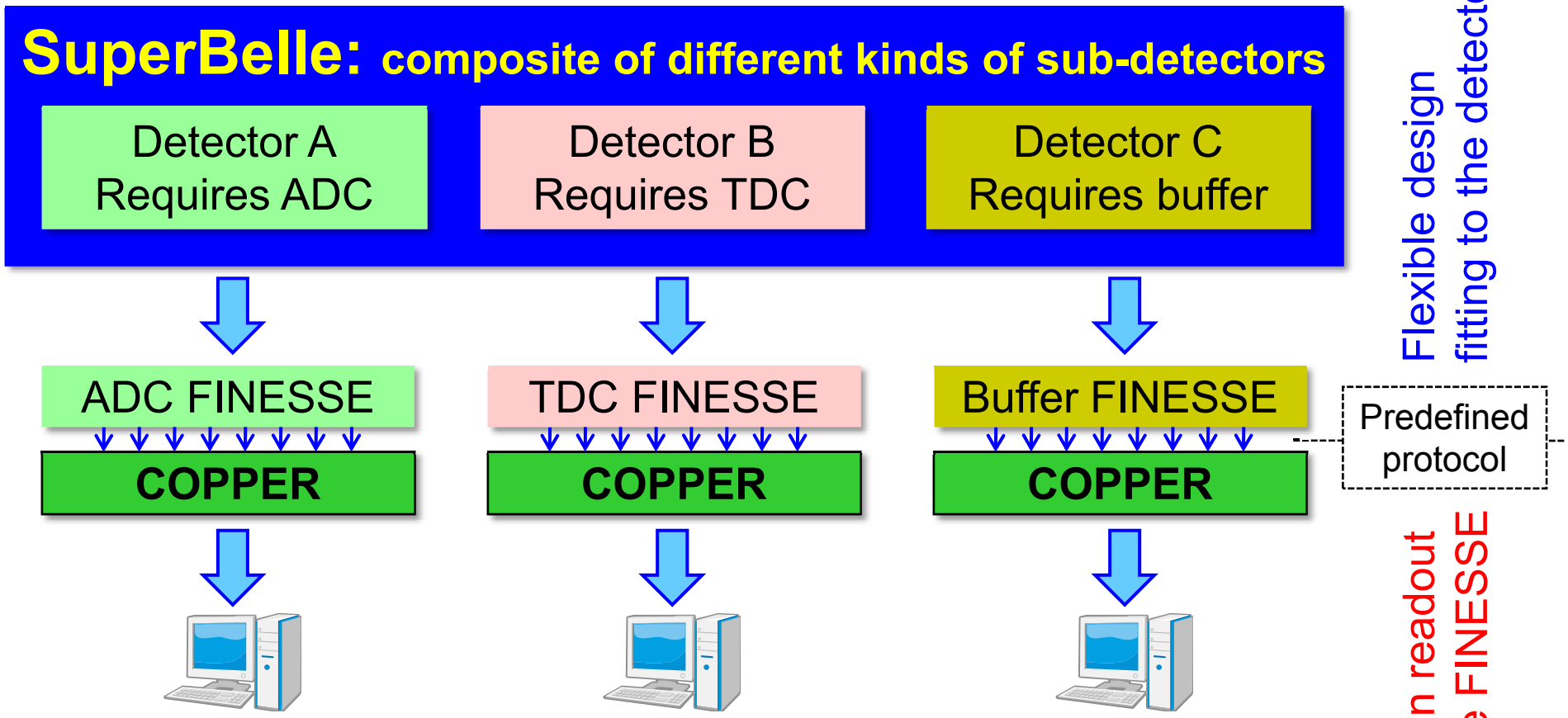
100BaseT port×2
Data transmission line and control line.

Trigger timing module
Add-on module to the COPPER. Responsible to receive trigger timing and system clock from upstream and to deliver them to the FINESSEs.

COPPER Block Diagram



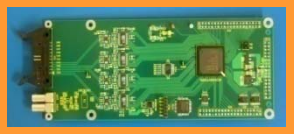
FINESSE



The COPPER/FINESSE system enables us/you to concentrate on the digitizer part without worrying about implementation of the readout part.

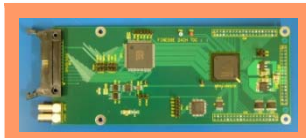
FINESSE Catalogue 2008

- **Several functions of FINESSEs are ready for hitchhikers.**

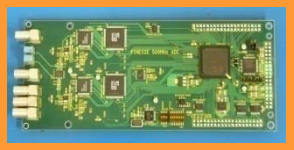


65 MHz 8ch FADC FINESSE

Digital Buffer FINESSE



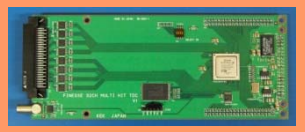
TDC FINESSE w/ AMT3 TDC chip



500 MHz 2ch FADC FINESSE

USB I/F FINESSE (Debug use)

TDC FINESSE w/ HPTDC chip



TDC FINESSE w/ Vertrx5 FPGA

Pixel Readout FINESSE

Dry run FINESSE

History of "Project COPPER"

- **2002-2003**
  - Start of design from a scratch.
  - First version of the COPPER.
- **2004**
  - Revision to the COPPER-II.
  - **Minimal performance study.**
- **2005**
  - Decision to replace entire Belle DAQ with the COPPER-II.
    - To reduce the DAQ deadtime, and
    - To make an *in-situ* system test toward SuperBelle.
  - **R&D of TDC FINESSE toward the DAQ replacement.**
  - Replacement of Belle EFC readout with the COPPER-II/ FINESSE (6).

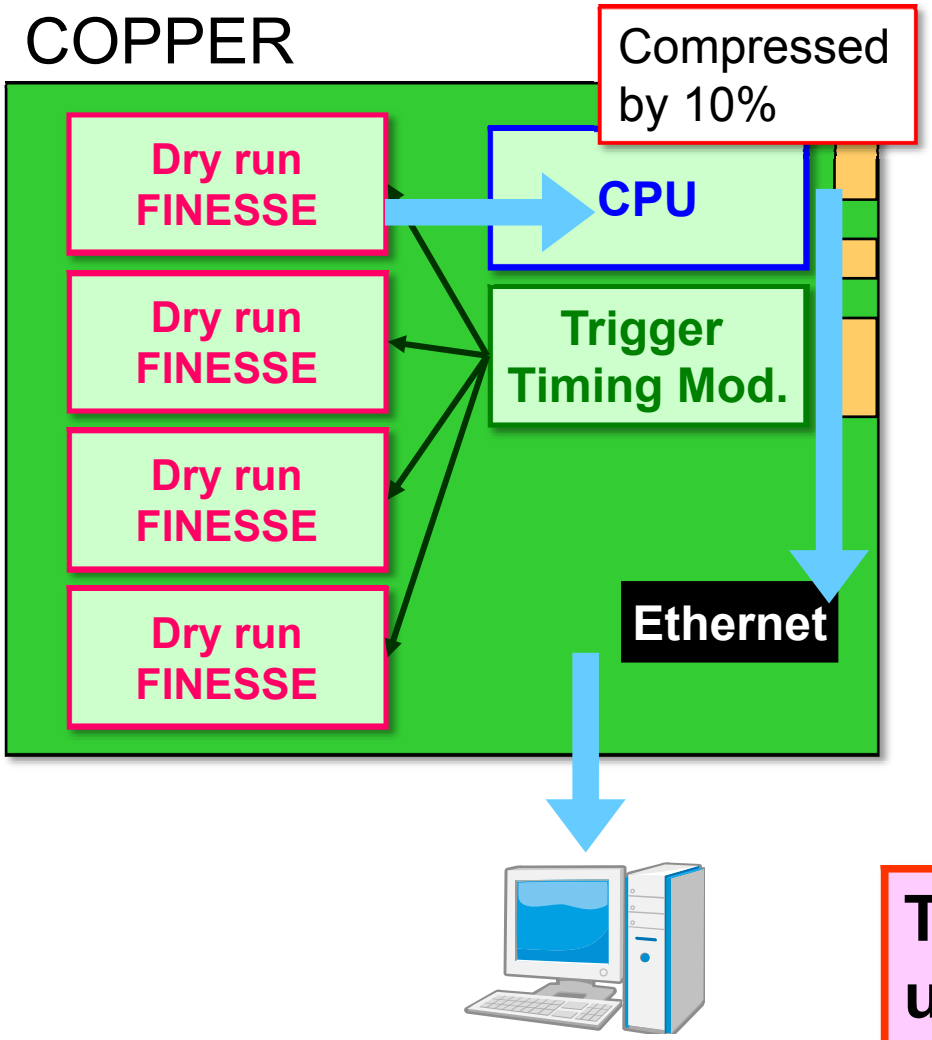
Red items will be described in detail later.

History of "Project COPPER"

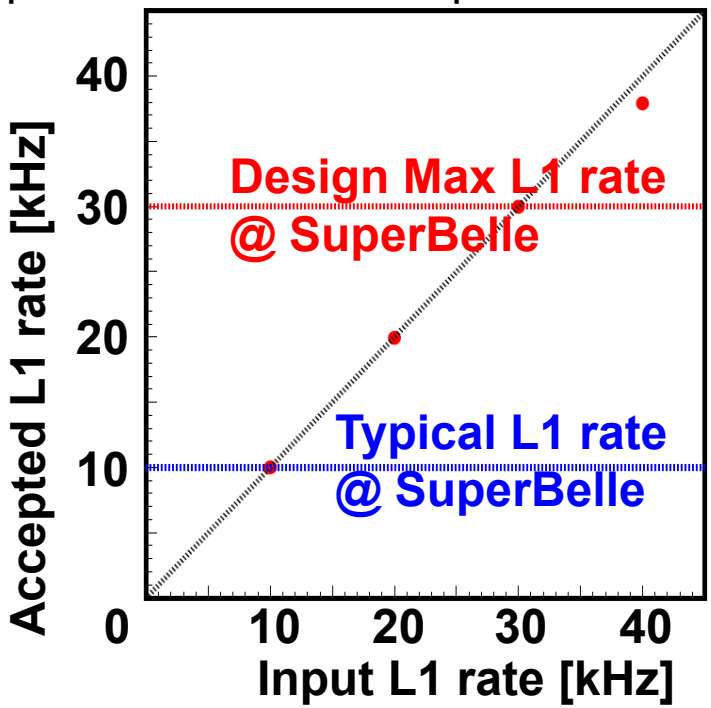
- **2006**
  - **System test in a full scale test bench.**
  - **Replacement of Belle CDC readout partially with the COPPER-II/FINESSE.**
  - **System test *in situ*.**

- **2007-2008**
  - **Replacement of Belle CDC readout with the COPPER-II/ FINESSE (89); intensive *in-situ* study.**
  - Replacement of Belle ACC readout with the COPPER-II/ FINESSE (24).
  - Replacement of Belle TRG readout with the COPPER-II/ FINESSE (26).
  - **Start of revision to the COPPER-3**.

Minimal Performance Study (2004)



@ 416 bytes/ev/FINESSE
(typical data size for SuperBelle CDC)

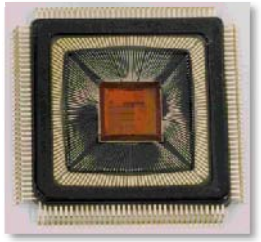


The COPPER works well even under the severest L1 rate (>30kHz) of the SuperBelle.

R&D of the TDC FINESSE (2005)

- **TDC chip selection = AMT3**

	Req.	AMT3
For tracking		
Position resolution	**< 130 um**	**27 μm**
For dE/dx measurement		
Dynamic range	**10 bit**	**17 bit**
Linearity	**< 0.5 – 1.0%**	**0.49%**
Other items		
Single rate	**200 kHz (?)**	
# of channels	**～15 k**	**24 ch/chip**



ATLAS
MUON
TDC

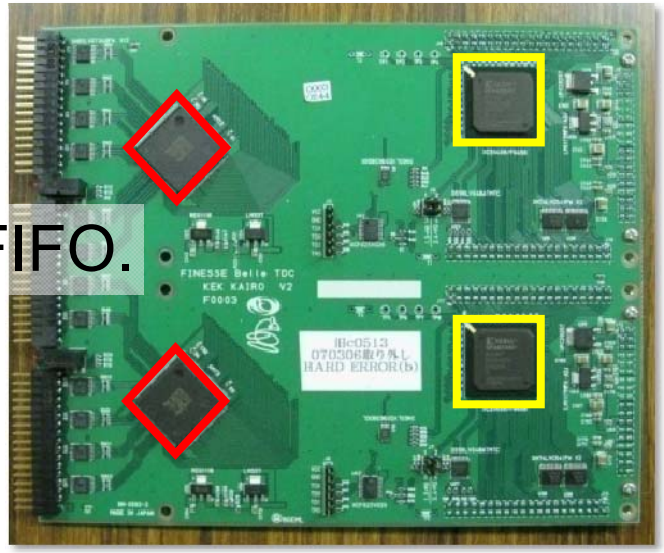
The AMT3 has a similar performance as the Belle FASTBUS TDC. It enables a seamless transition from the FASTBUS to the COPPER-II.

Equipped pipeline

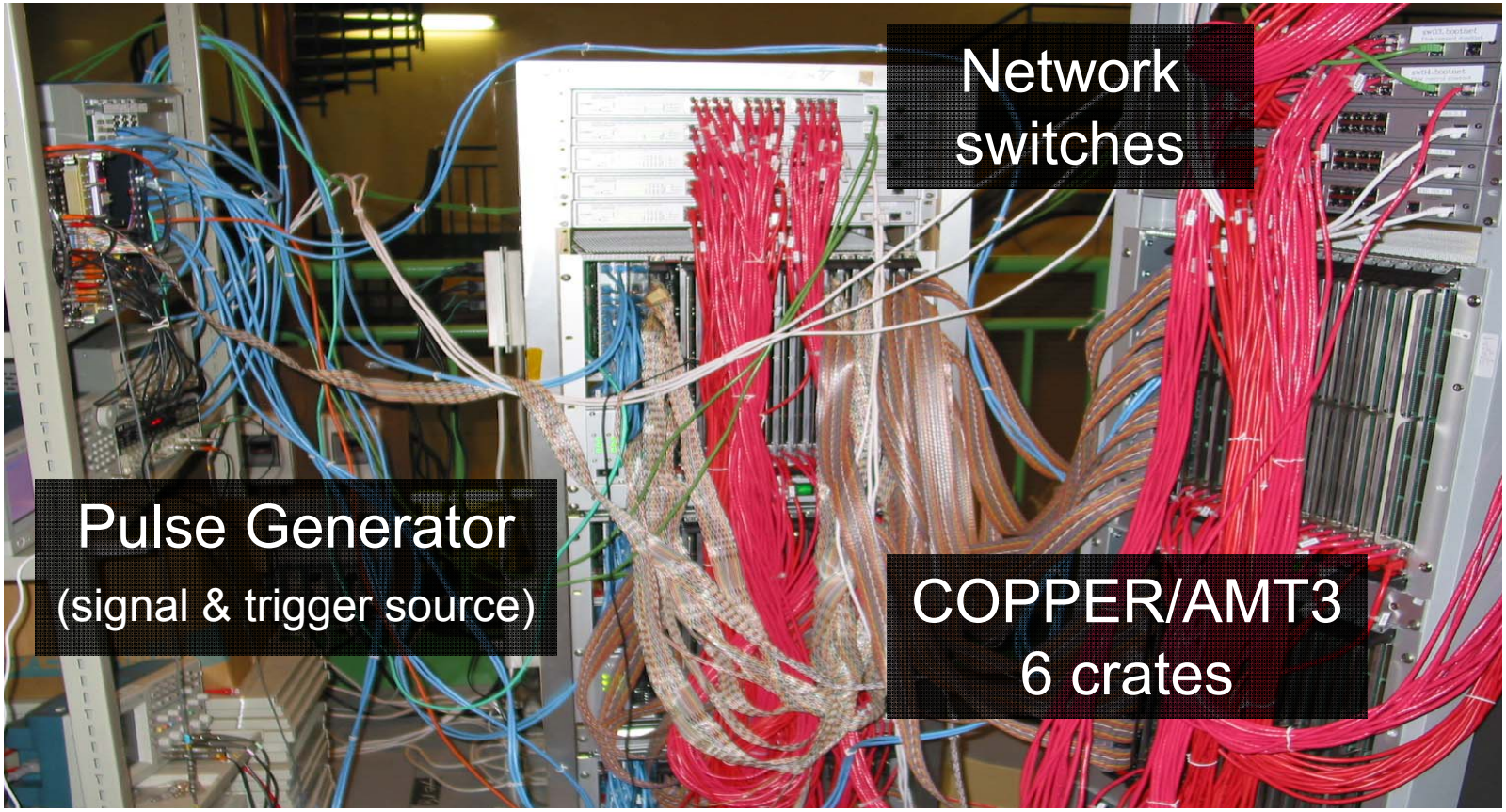
Channel buffer = **4 edges × 24ch**
L1 FIFO = **256 edges**
Readout FIFO = **64 edges**

AMT3 FINESSE (2005)

- **“Tandem” FINESSE**
  - FASTBUS TDC (manufactured by LeCroy) has 6 cable-connectors × 16 channels = 96 channels.
  - Not to change the cables configuration, we developed “tandem” FINESSE (occupying 2 slots), with 3 connectors.
- **AMT-3 TDC chip**
- **Spartan3 FPGA**
  - AMT3 register control.
  - Data readout from the AMT3 output FIFO.
  - Data formatting (header/footer etc.).
  - Data output to the COPPER FIFO.
  - I/F to the COPPER local bus.



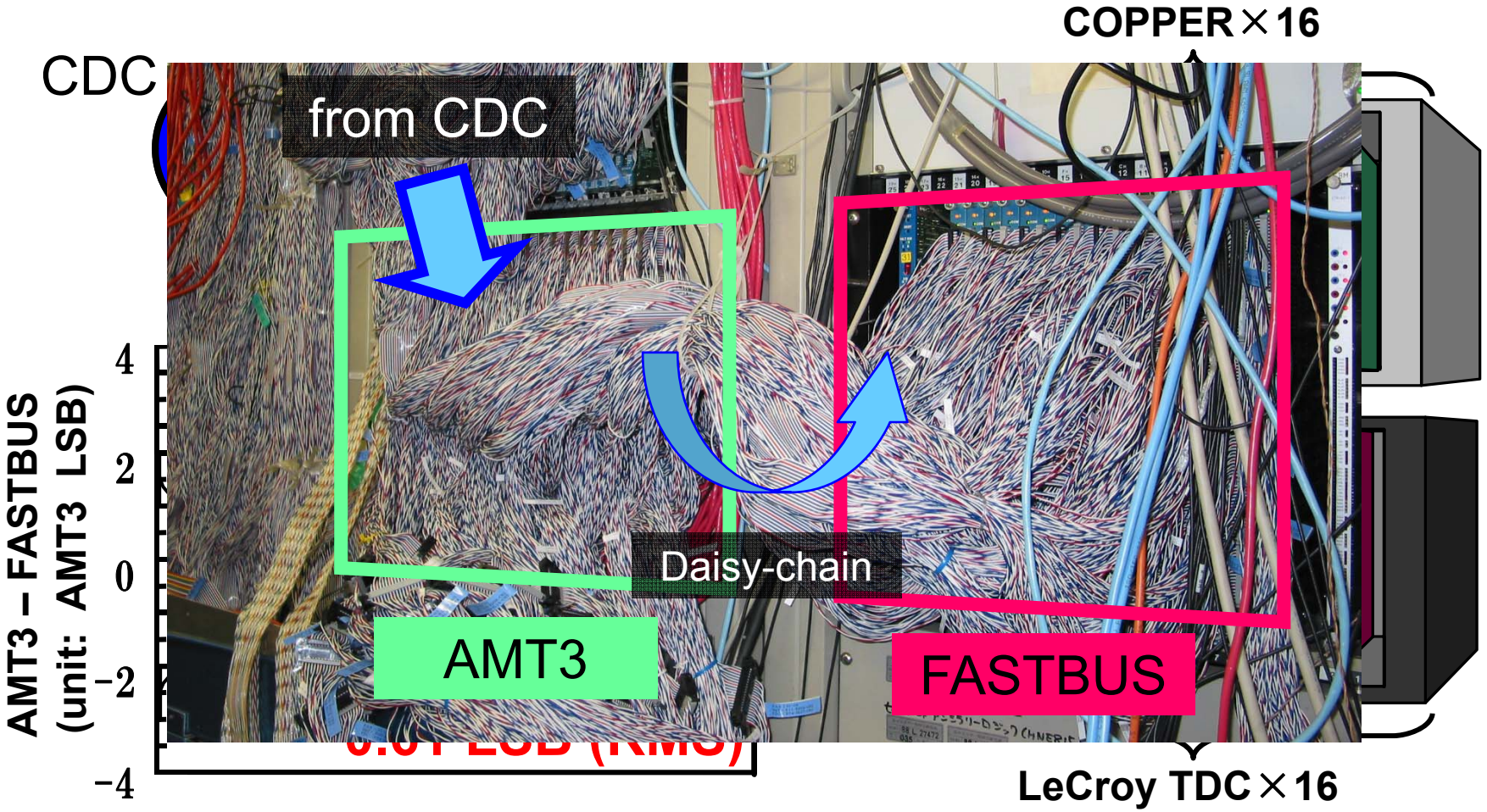
Full Scale Test Bench (2006 –)



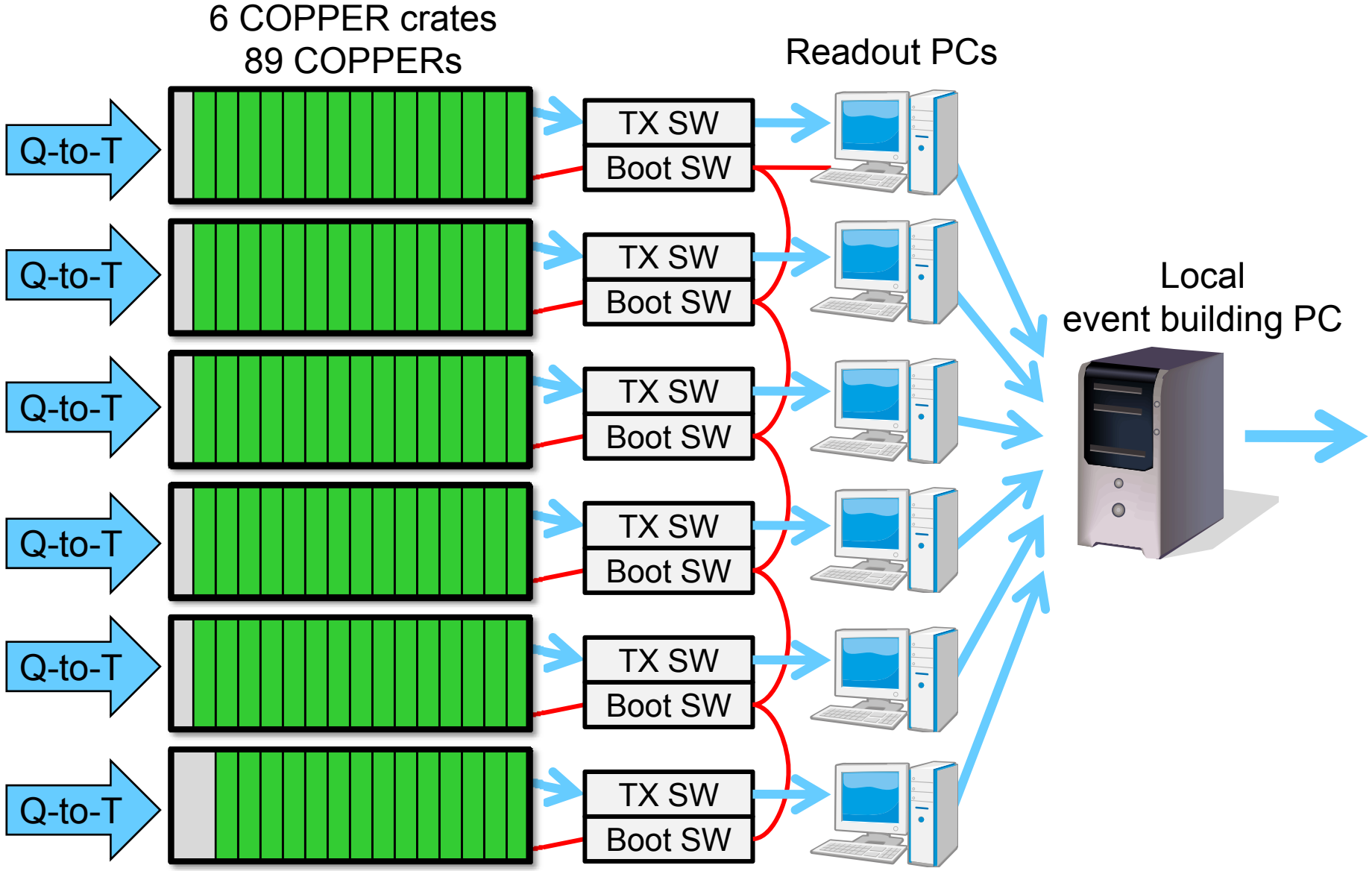
- Full-scale data flow simulation from the PG to the readout PCs.
- Detailed study of the AMT3 behavior (including debug).
- Establishment of the global control scheme.

In-Situ Study with Belle CDC (2006)

- **Word-by-word comparison of readout data by the FASTBUS and the COPPER-II/AMT3.**

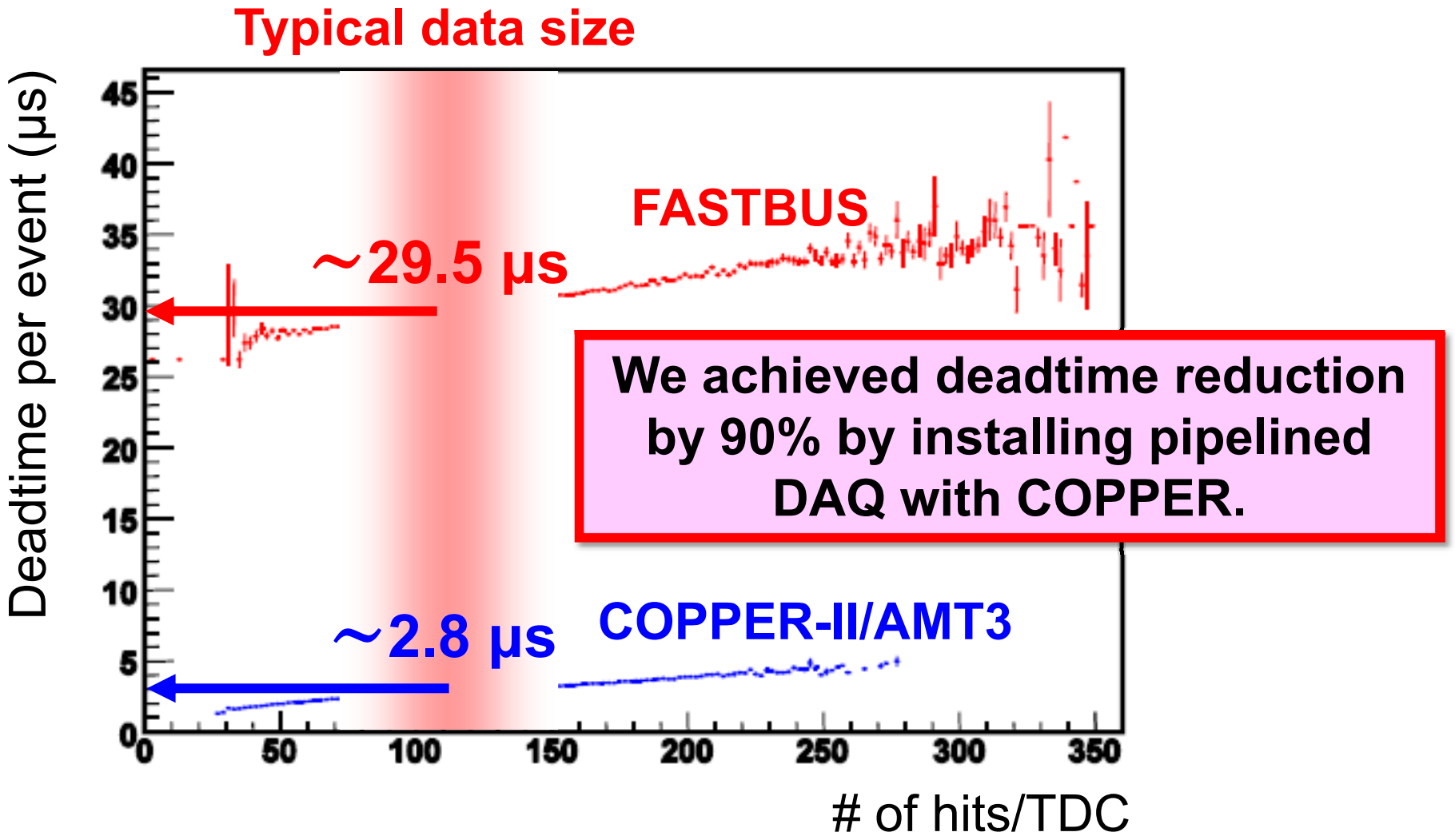


Full Replacement of CDC DAQ (2007)



Reduction of DAQ Deadtime (2007)

S.Y.Suzuki



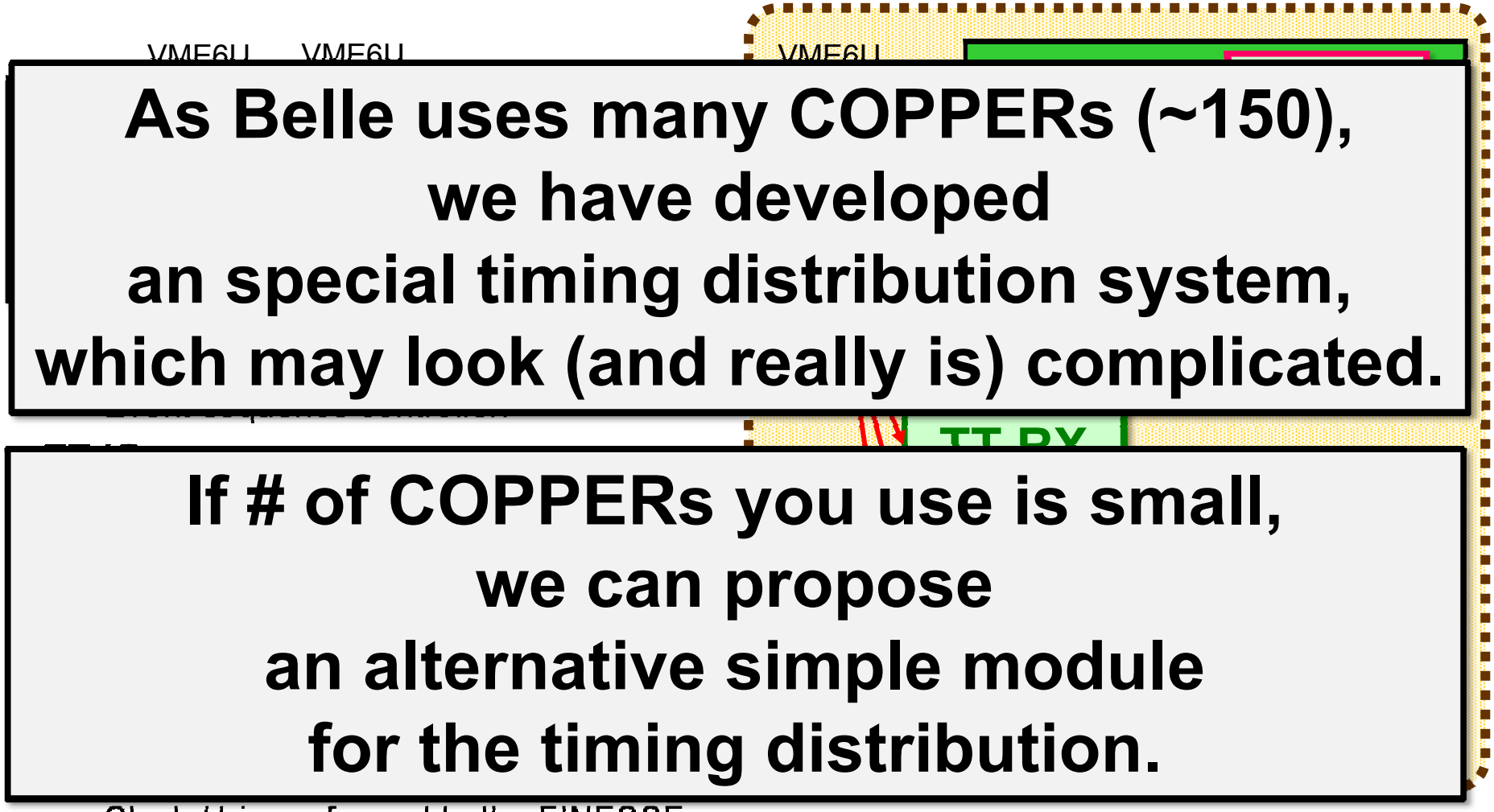
COPPER Is Not Difficult

- Several functions of FINESSEs are ready for you.
- Thanks to an excellent device driver, the COPPER can be read out quite easily.

```
int main(int c, char *v[])
{
  int fd;

  fd = open("/dev/copper", O_RDONLY);

  /* put your FINESSE initialization here */

  while(1){
    static char buf[1024*1024];
    read(fd, buf, sizeof(buf)); /* data read */
  }
}
```

That's all.

Timing Distribution for COPPER



As Belle uses many COPPERs (~150), we have developed an special timing distribution system, which may look (and really is) complicated.

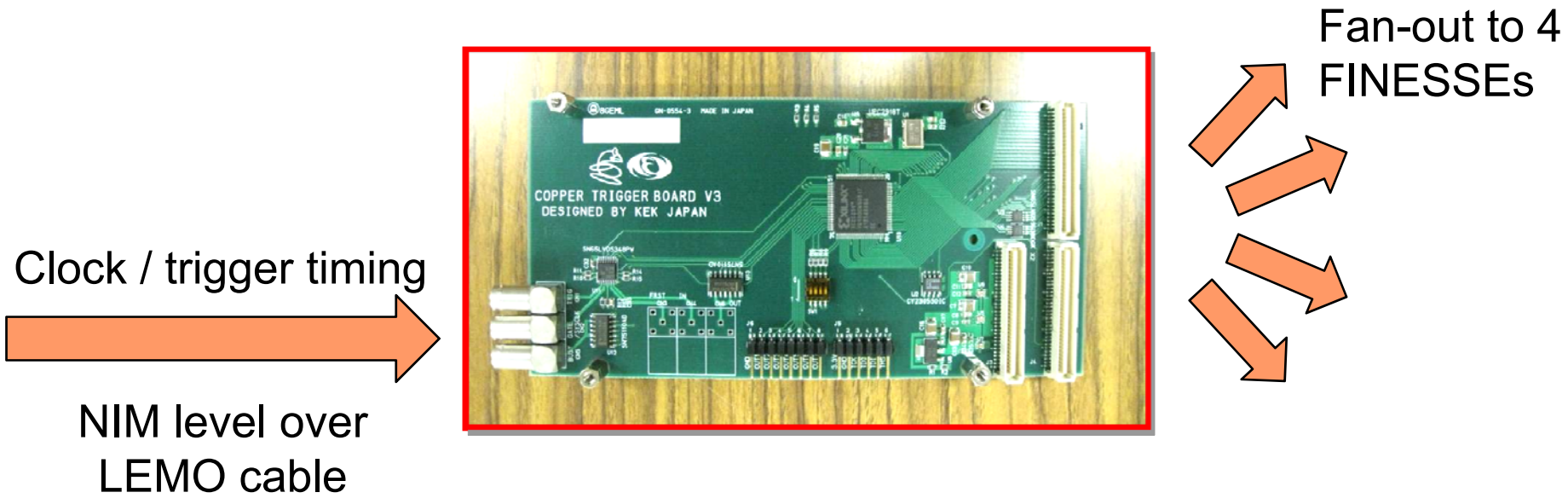
If # of COPPERs you use is small, we can propose an alternative simple module for the timing distribution.

- Clock / trigger fan-out to the FINESSEs.
- Busy collection from FINESSEs.

M.Nakao

COPPER Is Not Difficult

- **"Simple trigger board" plugged on the COPPER**
  - Suitable for a compact experiment.



Y.Igarashi, K.Tauchi

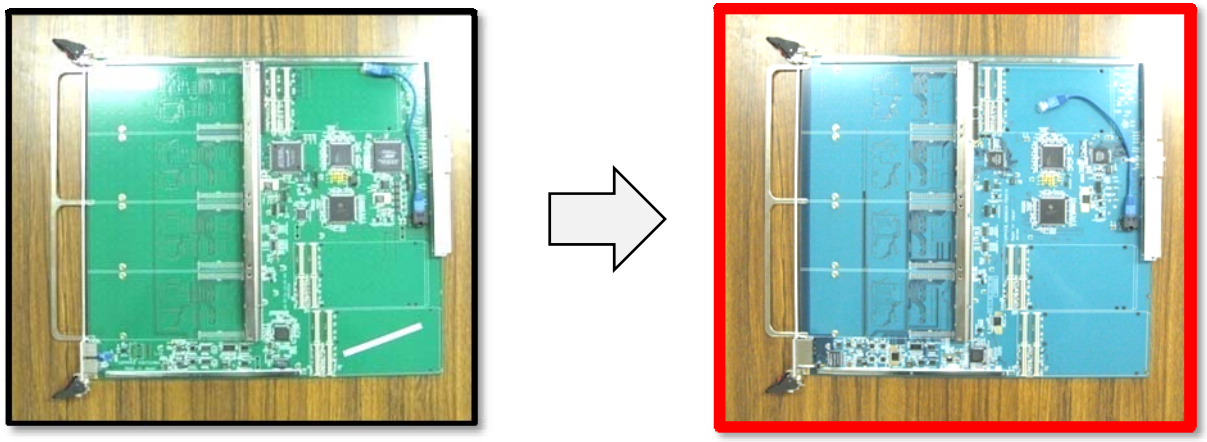
COPPER Users

- **Belle:** **Half of the DAQ is COPPER'ized**
- **SuperBelle:** **Planning to utilize the COPPER.**
- **T2K:** **Beam monitor**
- **muSR**
- ***and YOU***

Please join us and enjoy data taking with the COPPER system.

COPPER-3

- **COPPER-II → COPPER-3**
  - Replacement of terminating parts with recent ones.
  - Fix jumper patches by pattern layout.
  - Upgrade onboard Ethernet chip to Gbit-Ethernet.
  - and others.

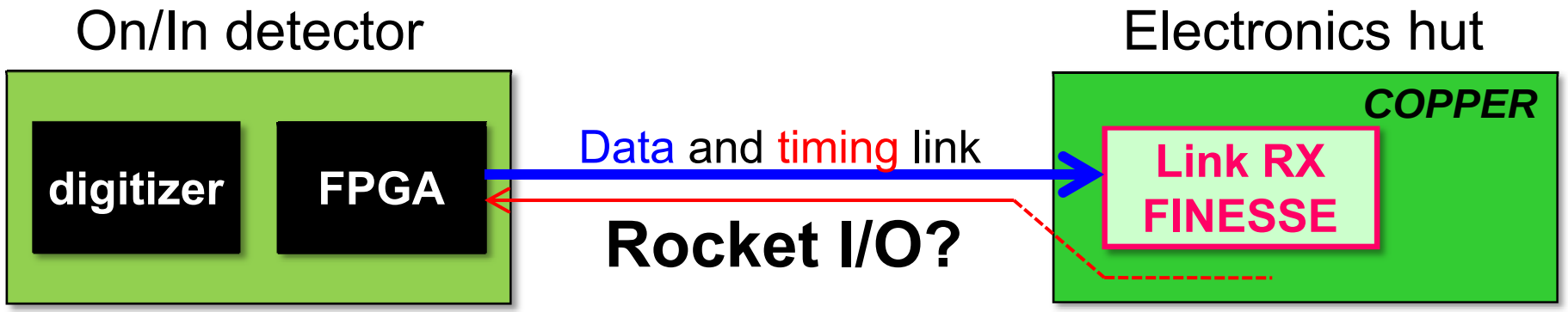


- **We confirmed the COPPER-3 is fully compatible with the COPPER-II using AMT3 FINESSE.**

Brief Prospects of SuperBelle DAQ

- **Preliminary design**

Detector	Digitizer	Location	FPGA link	FINESSE
Pixel	?	On hybrid	Yes	Link RX
SVD	APV25	EH	–	Special
CDC	ASD based	In detector	Yes	Link RX
RICH/TOP	Special ASIC	In detector	Yes	Link RX
ECL	Waveform Sa.	On detector	Yes	Link RX
KLM	?	In detector	Yes	Link RX



Summary

- We developed a new readout system “COPPER” toward the higher luminosity HEP experiment.
- We developed a TDC FINESSE equipped with an AMT3 chip to readout the Belle CDC; In the *in-situ* study, we found the COPPER/FINESSE/AMT3 system showed high compatibility to the FASTBUS DAQ system.
- The COPPER is quite easy to operate. We introduce you to join us and to be a member of COPPER user team.
- We are designing COPPER-3.
- Design of a new FINESSE for SuperBelle has also been started. In SuperBelle, one of key roles of the FINESSE will be data RX.