Muon trigger electronics development toward high luminosity LHC

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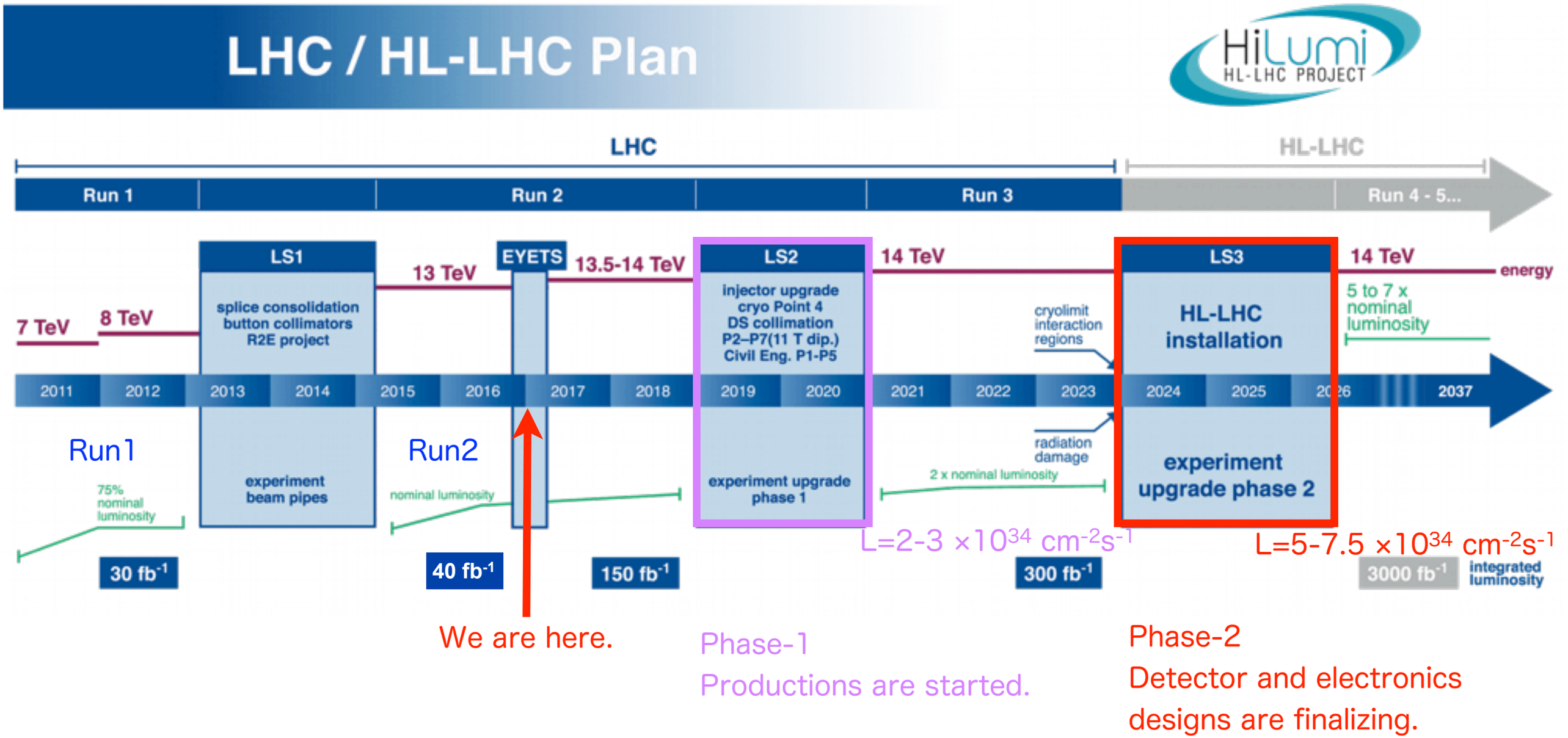
Introduction

- LHC is the energy-frontier experiment to explore new physics by :
  - precise measurements of Higgs couplings and the other SM processes, and
  - direct searches for new particles and phenomena

- A series of LHC accelerator and ATLAS detector upgrades are scheduled.



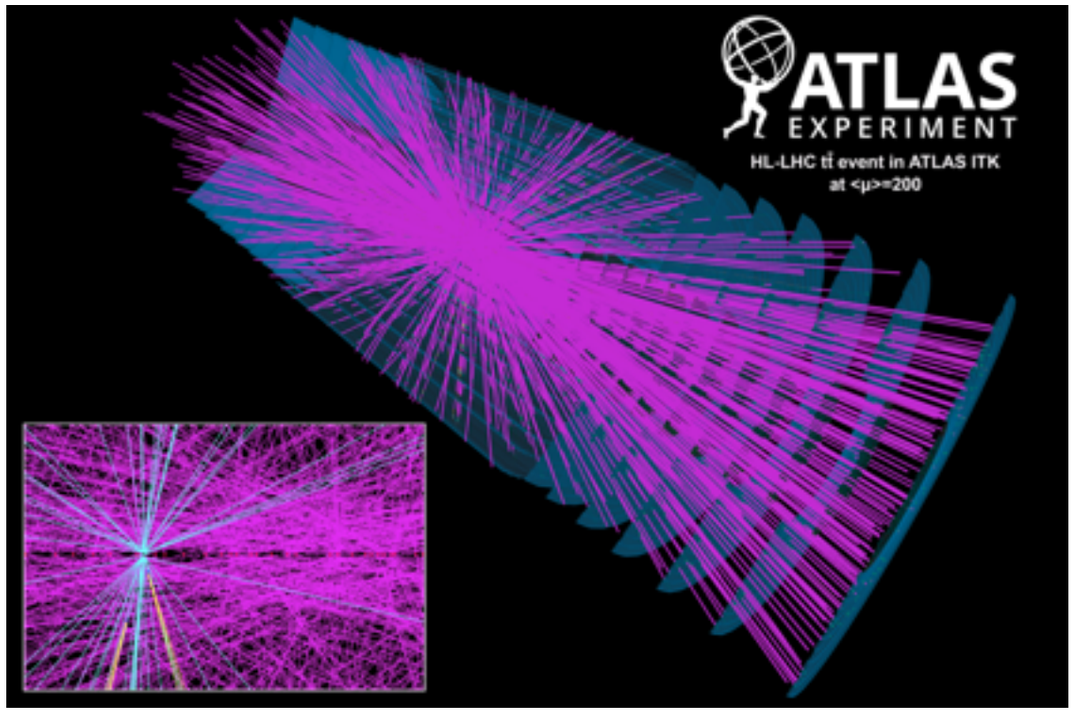
We are here.

Phase-1
Productions are started.

Phase-2
Detector and electronics designs are finalizing.

Phase-2 upgrades

- The detector for HL-LHC should be designed for peak luminosity of 7×10^{34} cm^{-2} s^{-1} and integrated luminosity of 3000 fb^{-1} (300 fb^{-1}/year).
  - The rates for low-q^2 QCD background events are increased.
  - The average number of collisions per bunch crossing (pileup) is the level of 200.
  - The detector and electronics are exposed to more intense radiation.



A top quark pair production event with 200 collisions (pileup)

- The detector upgrade for HL-LHC is focused on
  - Development of the advanced trigger and data acquisition system

  ➡Muon trigger upgrade

  - Replacement of the inner and forward detectors

  ➡Inner tracker upgrade

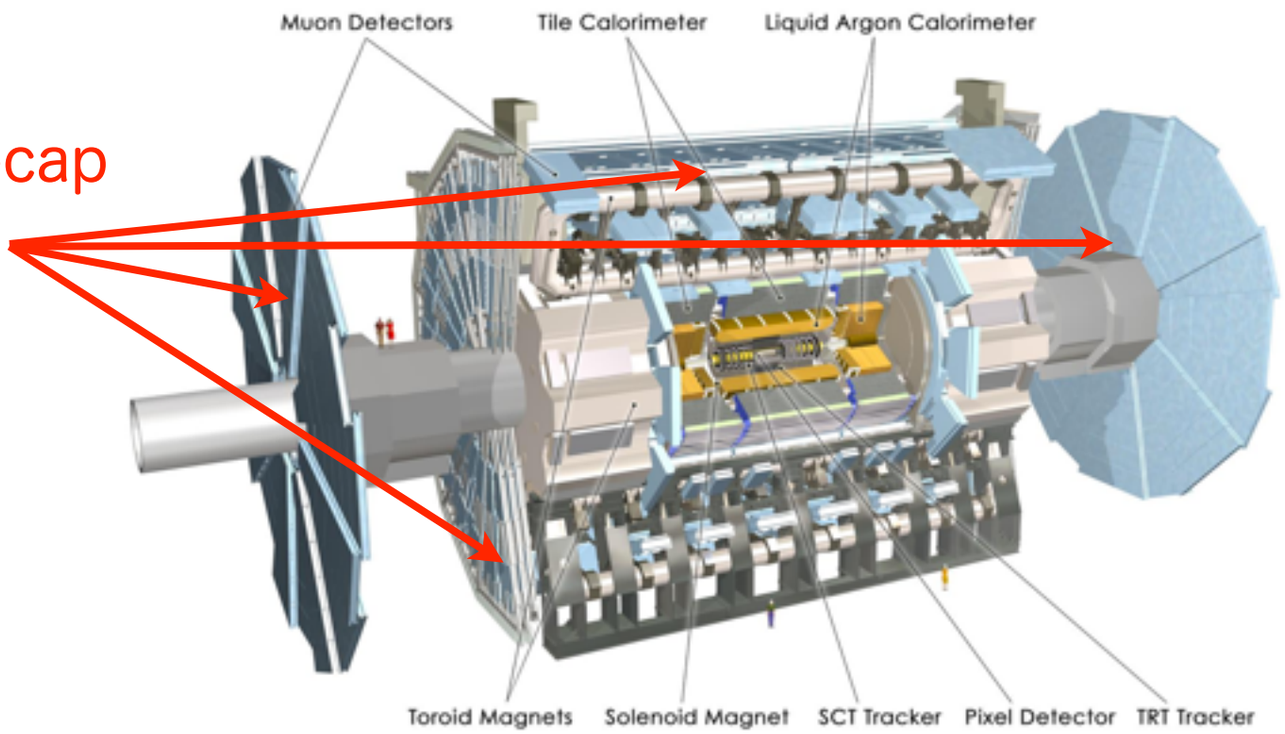
Trigger and readout scheme

- To take full advantage of HL-LHC, a new trigger and readout scheme with longer latency and higher rate is essential.

	Latency	Rate
Current	2.5 μs	100 kHz
HL-LHC	10 μs	1 MHz

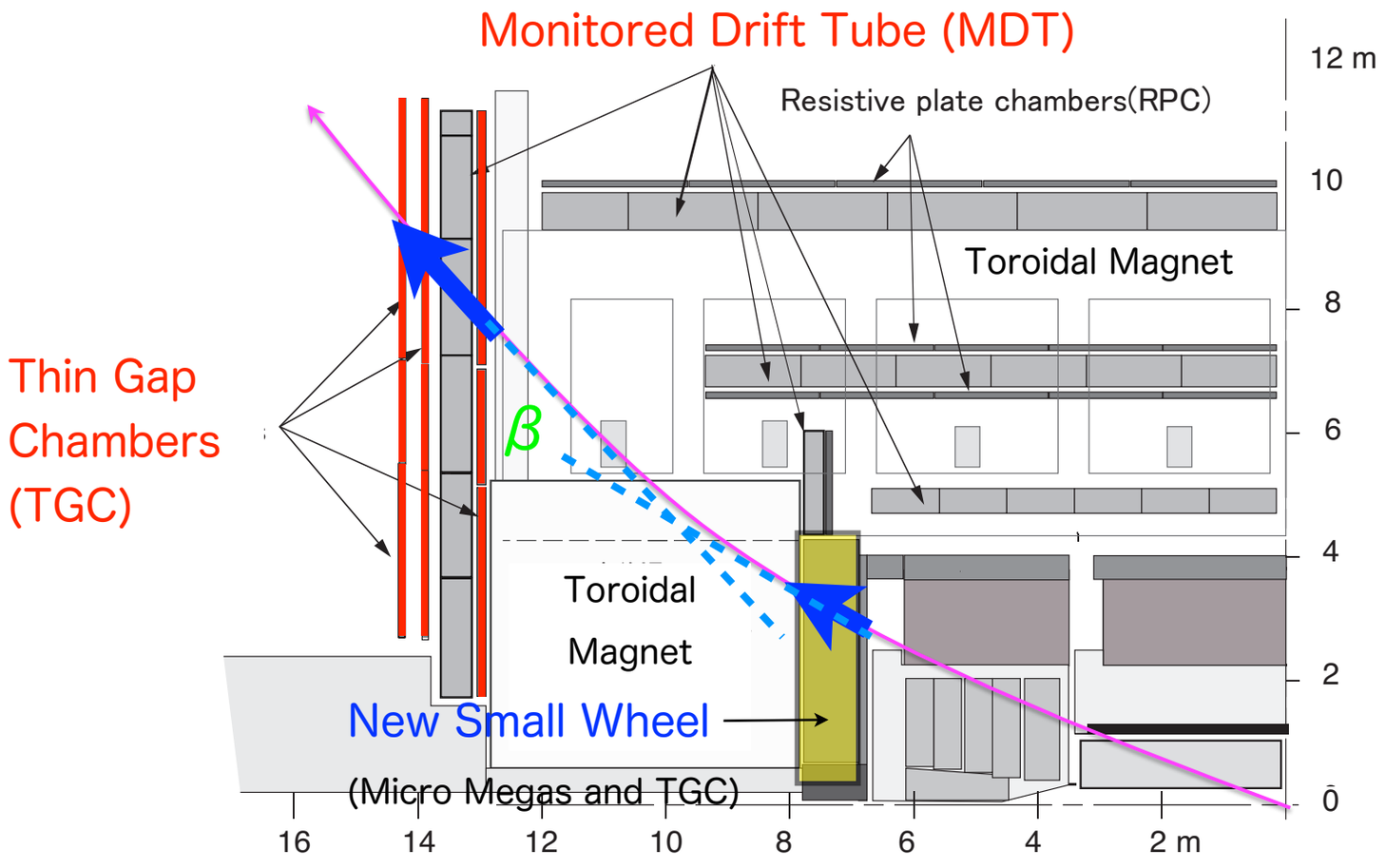
- Most of the electronics for muon system should be replaced by new ones.
- The advanced muon trigger algorithm is developed to reduce the background rate with keeping the efficiency of the interesting events high.
  - Coincidence trigger → Tracking trigger

Muon detectors :
Monitored drift tube (MDT): barrel & end-cap
Resistive plate chamber (RPC): barrel
Thin gap chamber (TGC): end-cap



End-cap muon trigger upgrade

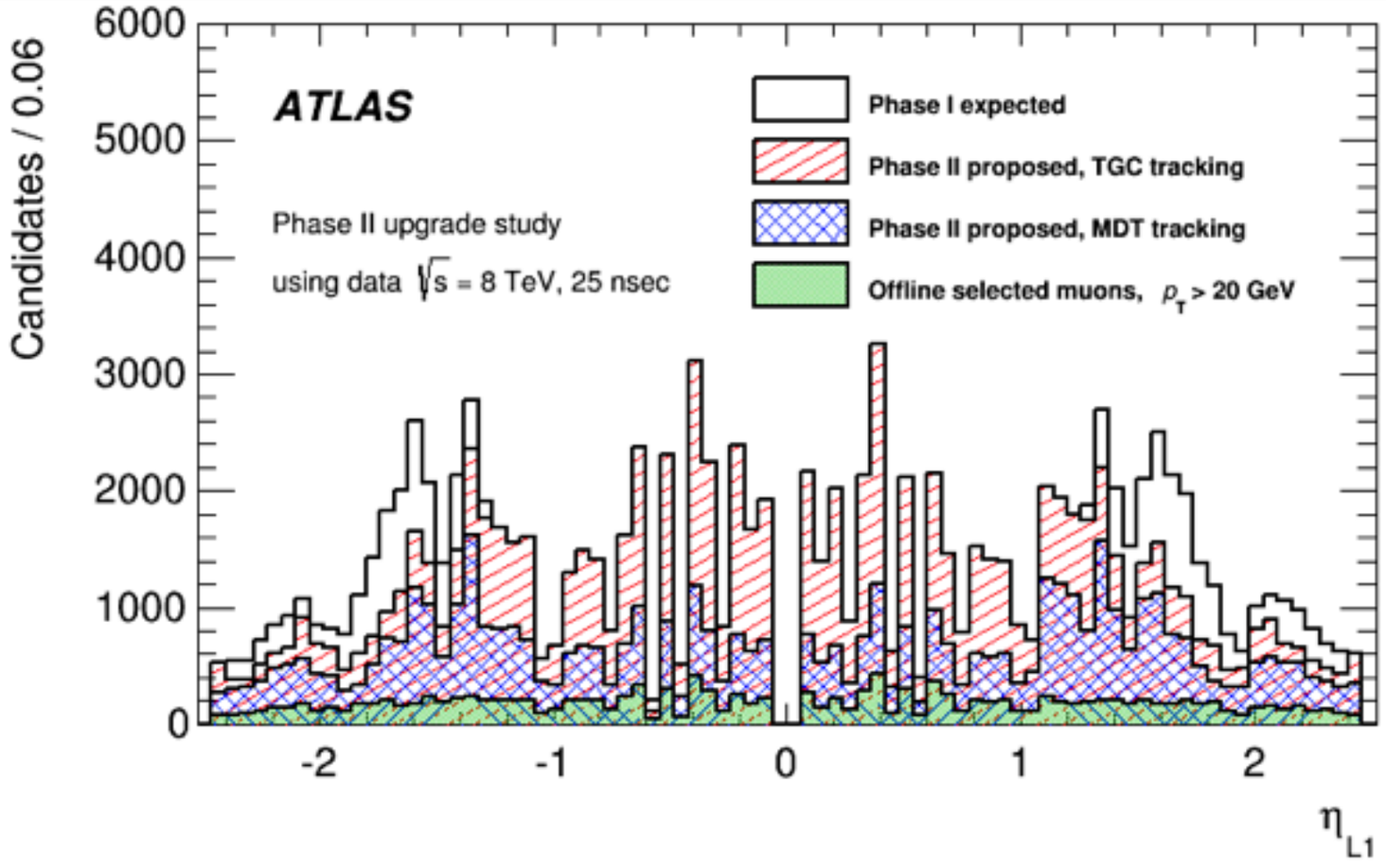
- In HL-LHC, the end-cap muon trigger makes trigger decision using the deflection angle (β) between track segments provided by the inner and outer stations
  - New small wheel (introduced after the Phase1 upgrade) will provide the track segments with ~1 mrad resolution.
  - Upgraded TGC trigger will provide the track segments with ~3 mrad resolution.
  - MDT trigger will be newly introduced from Phase2 upgrade and provide the track segments with ~1 mrad resolution.

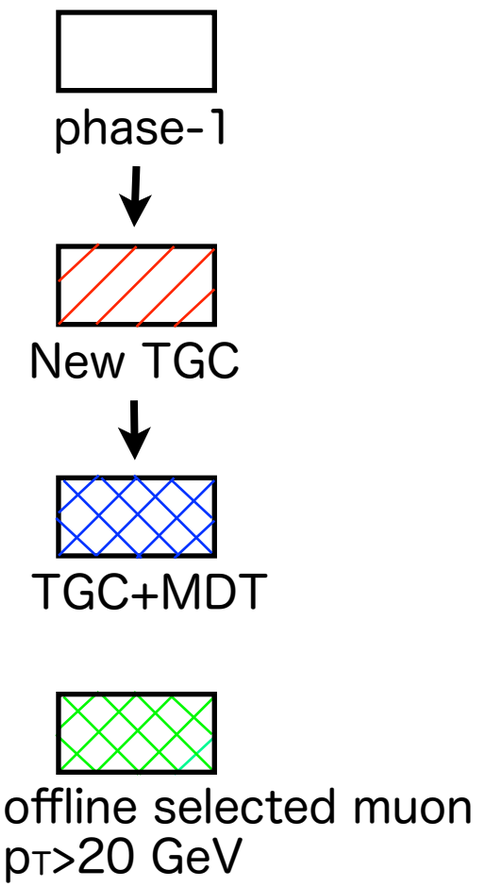


Performance of new muon trigger

- Trigger rate study for single muon trigger with 20 GeV threshold is emulated using Run1 data, $\sqrt{s}$=8 TeV, 25 ns bunch spacing
  - Rate reduction by the TGC tracking trigger is about 30% in end-cap region ($1.3 < |\eta| < 2.4$)
  - Rate reduction by the combination of the TGC tracking trigger and the MDT tracking trigger is about 50% in $|\eta| < 2.4$
  - Efficiency of muons reconstructed as p_T>20 GeV by offline is better than 95%

η distribution of the muons passed the muon trigger condition of p_T > 20 GeV

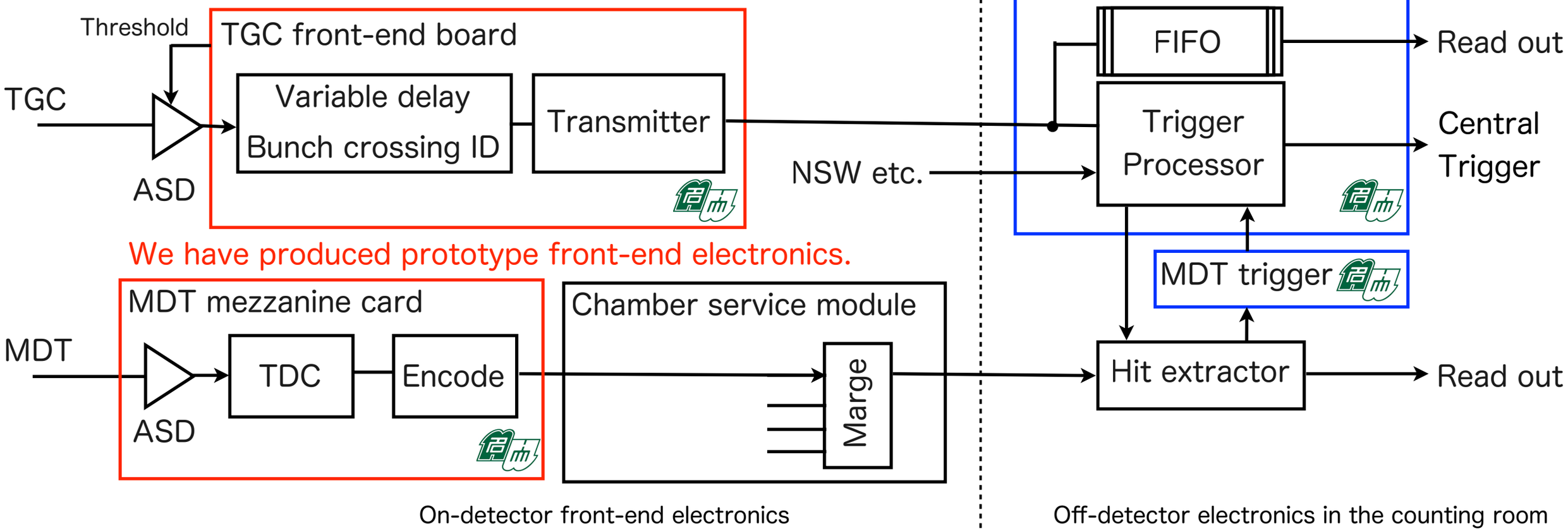




End-cap muon track trigger electronics

ASD=amplifier-shaper-discriminator ASIC

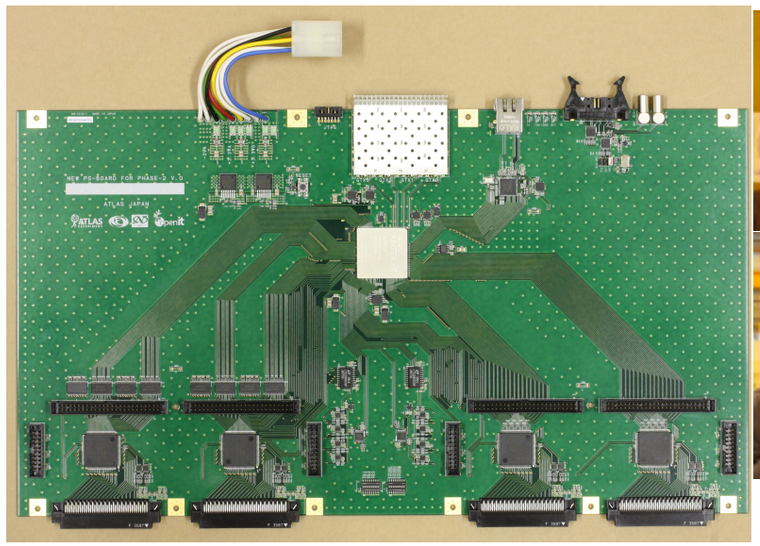
We are developing trigger algorithm.

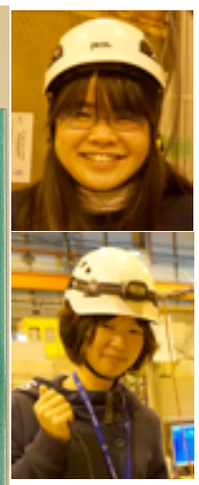


On-detector front-end electronics

Off-detector electronics in the counting room

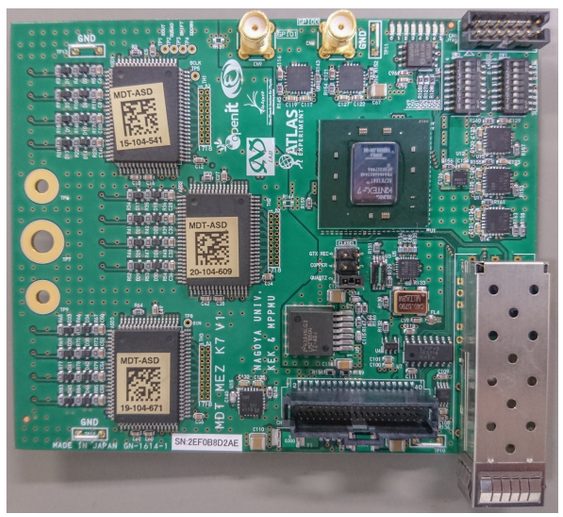
TGC front-end board
(20 Gbps hit data transmitter, discriminator threshold)

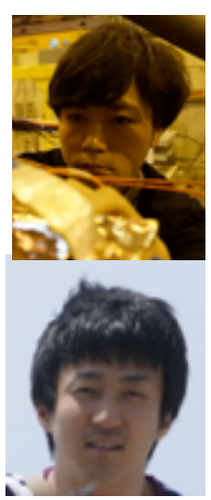




K. Shukutani
T. Kawaguchi

MDT mezzanine card
(TDC readout of drift tube signal)



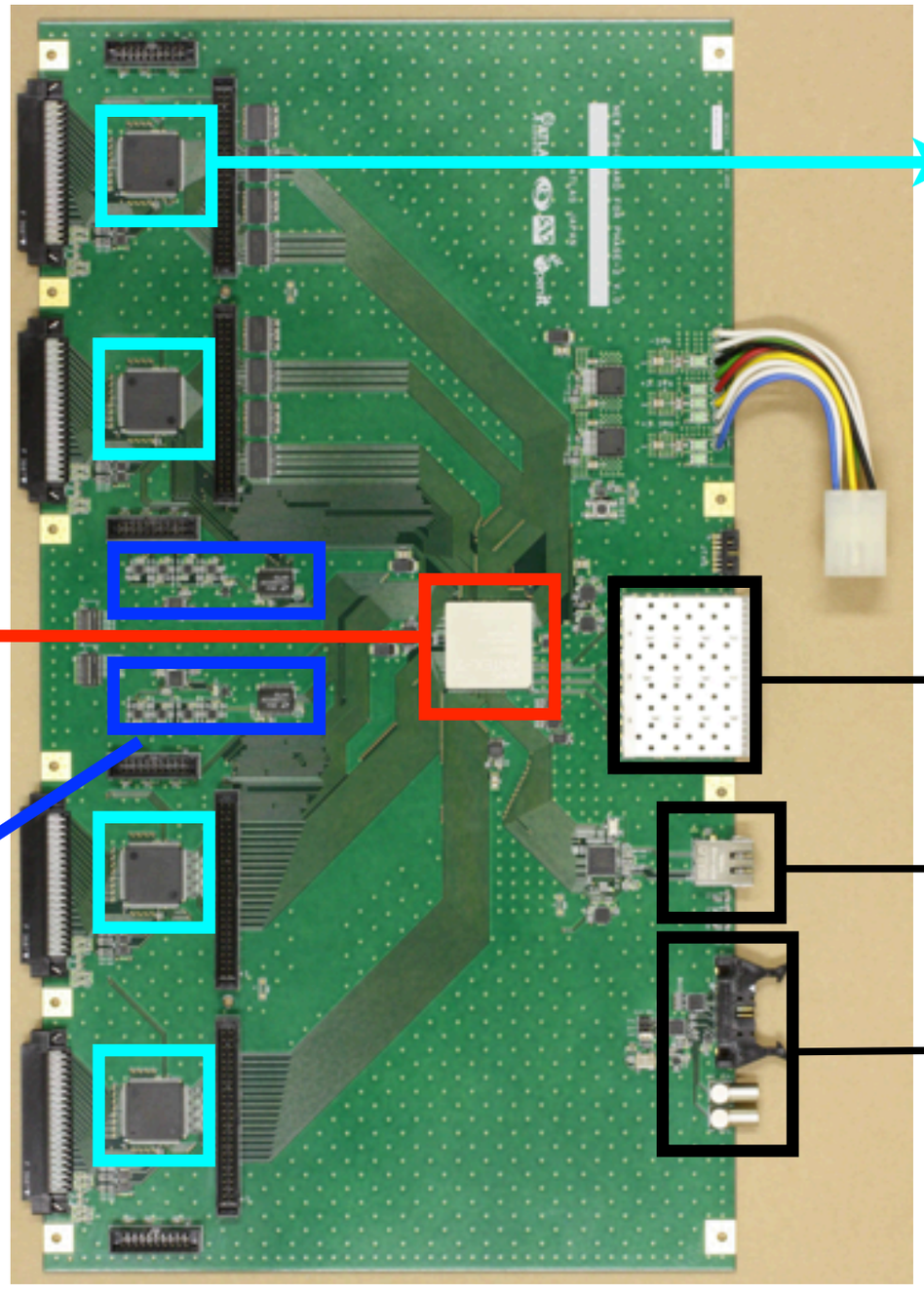


K. Mizukoshi
Y. Horii

Prototype of TGC front-end board

256 channels

450 mm × 270 mm



Bunch crossing ID ASIC
8 ASICs
4 on mother board
4 on daughter board

FPGA
Xilinx Kintex-7
(XC7K325TFFG900)
TGC data Transmitter
ASIC/DAC/ADC control

SFP+ connectors
4 Tx and 4 Rx
(up to 40 Gbps)

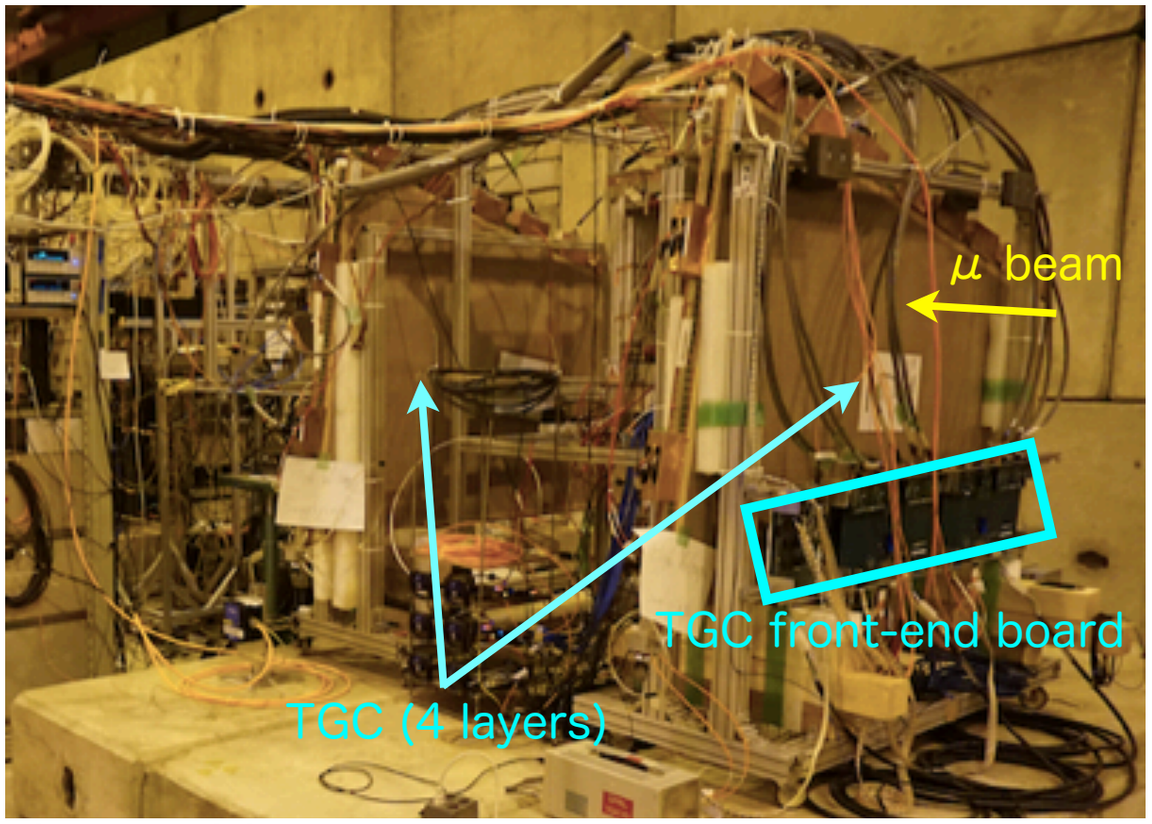
DAC
DAC7578SPW
ADC
LTC1289CCSW

RJ45 connector
for debugging

External clock etc.

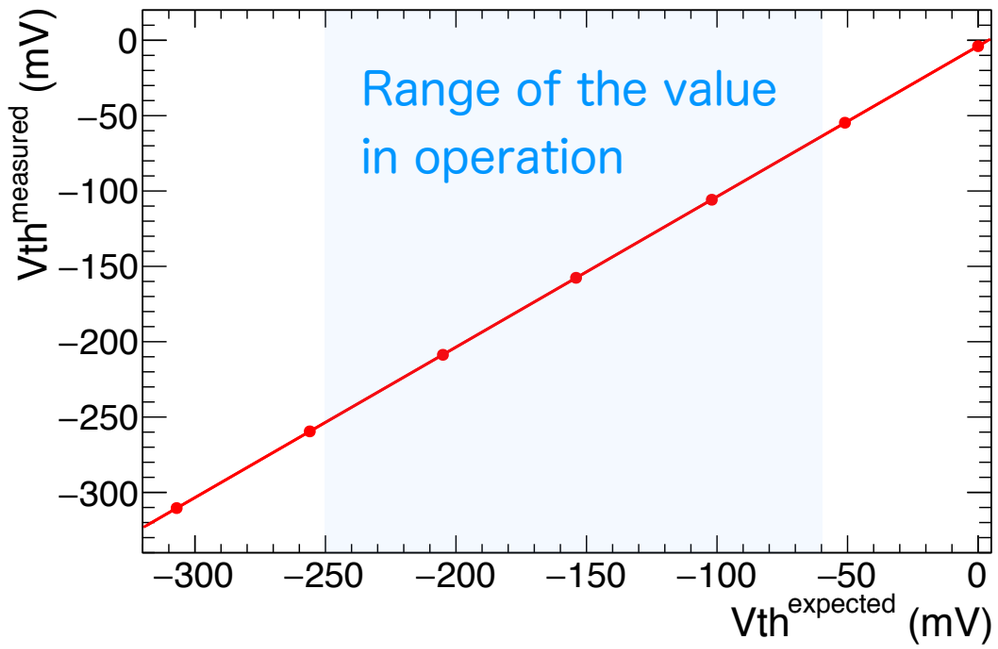
- This board has all functions for HL-LHC upgrade.
  - Bunch crossing ID ASICs need to be replaced by new ones.
  - Operating devices (FPGA etc.) in the intense radiation needs to be tested.

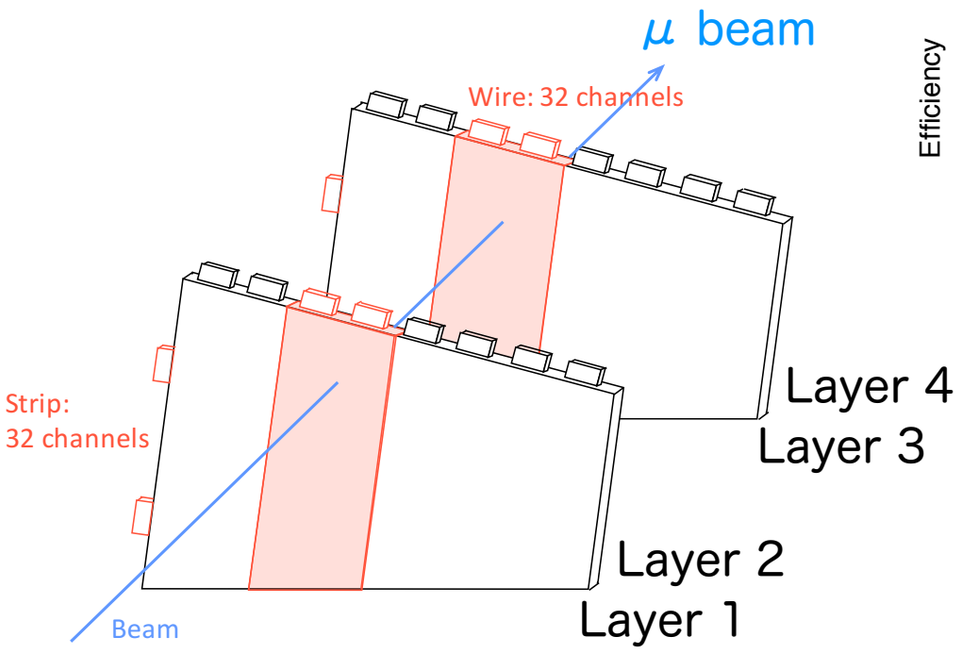
Demonstration of TGC front-end board with test beam



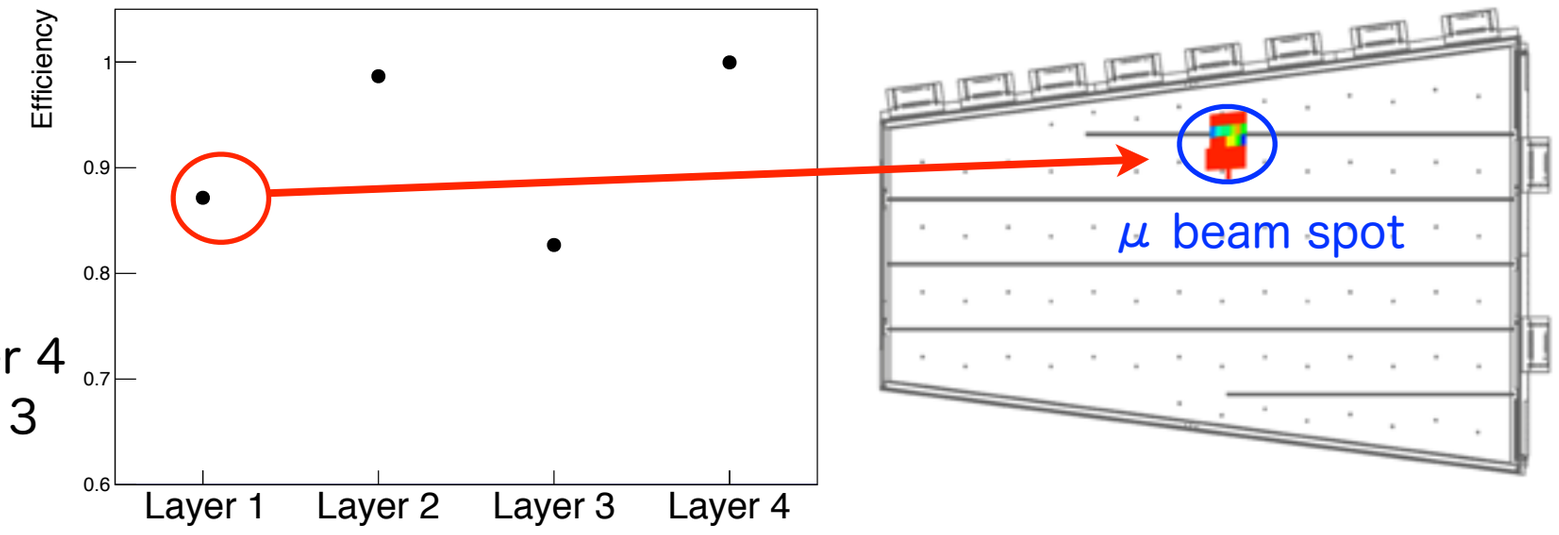
CERN H8C beam line

Linearity of DAC for the discriminator threshold





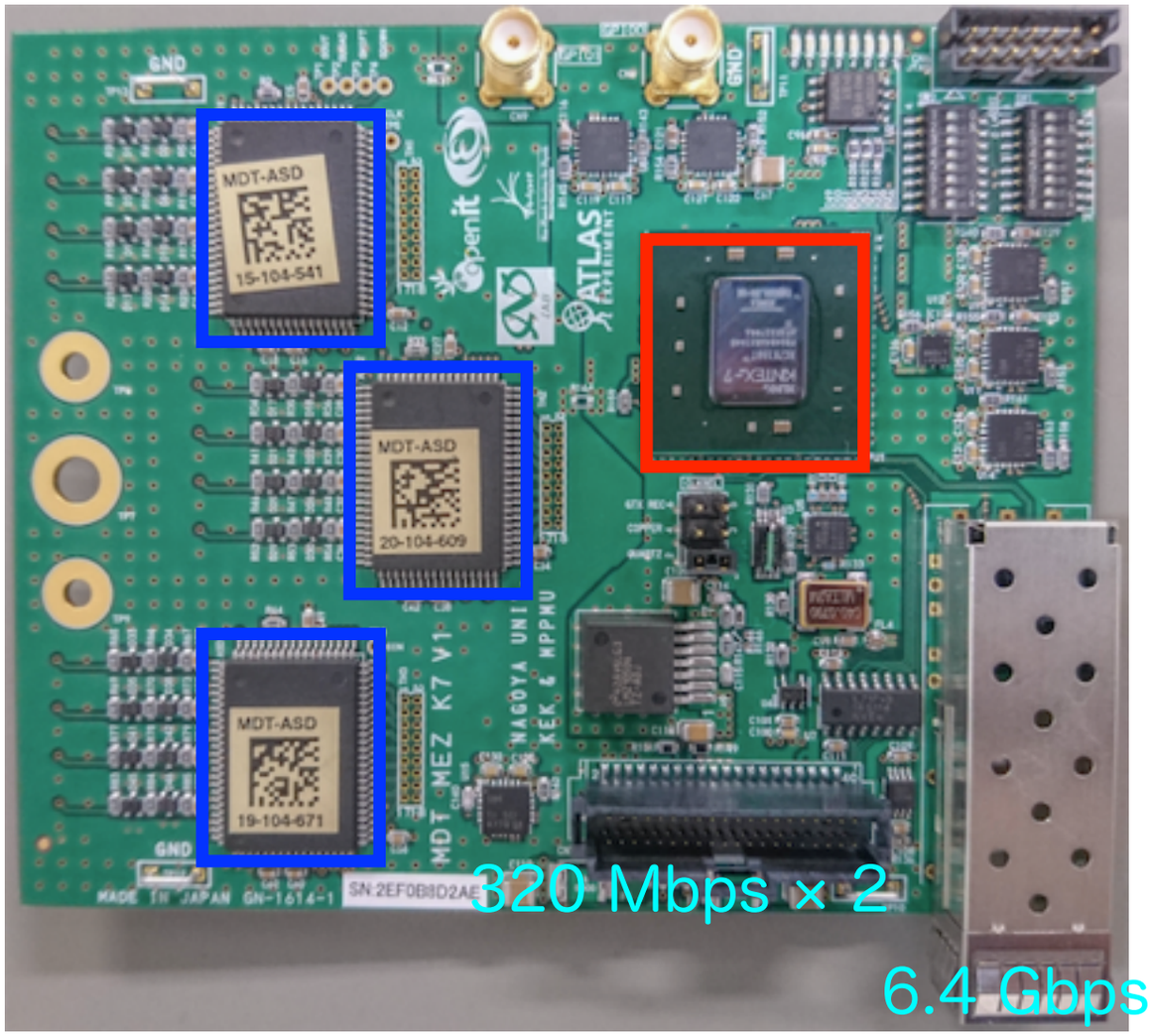
Efficiency of TGC hits



The efficiencies for L1 and 3 are lower due to the support structure.

The basic functionalities of TGC front-end board has been demonstrated.

Prototype of MDT mezzanine card

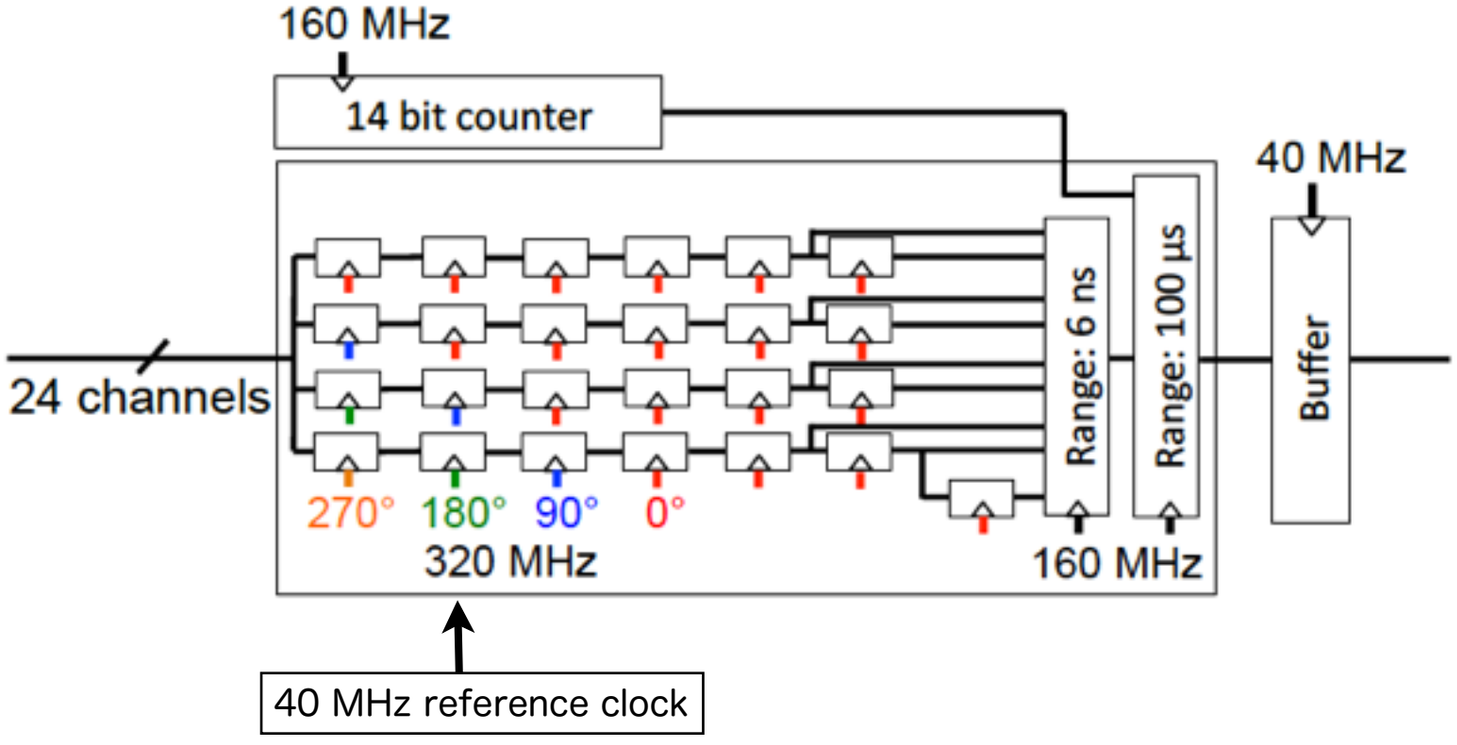


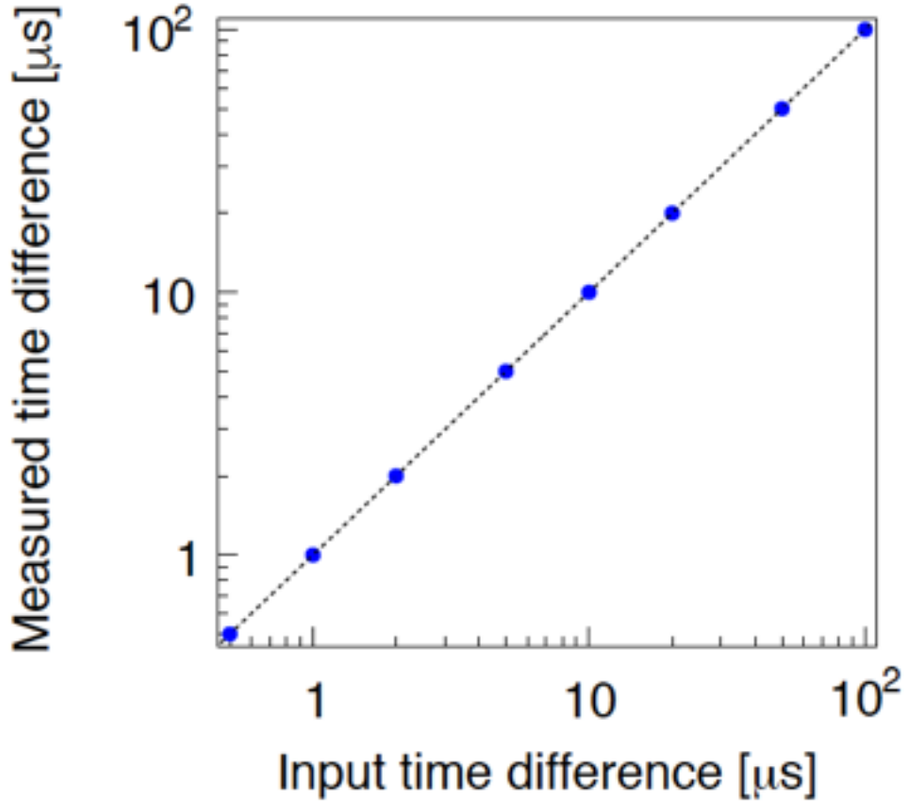
- 24 channels
- 112.9 mm × 92.71 mm
- Chips
  - 3 ASD (amp-shaper-discriminator) ASIC
  - 1 Kintex-7 FPGA (Xilinx) for TDC
- I/O
  - 3 Input connectors for input (other side)
  - 1 LVDS copper connector for output
  - SFP+ connector (6.4 Gbps) for debug
  - 2 SMA connectors

- This board has all functions for HL-LHC upgrade.
  - ASD ASIC needs to be replaced by new one (developed by MPI group).
  - Radiation-tolerant TDC device needs to be considered.
    - We are testing to operate FPGA in the intense radiation.
    - Alternative candidate is the MDT mezzanine card with ASIC TDC (proposed by US group)

TDC on FPGA

- A multisampling scheme using quad phase clocks with frequency of 320 MHz is employed to make the bin size of 0.78 nsec.
- The quad phase clocks are synchronized with 40 MHz reference clock (from LHC).
- Time resolution is measured using the test pulse to be 0.23 nsec
  = quantization error (0.78 /√12)
- The linearity from 0.5 μsec to 100μs is confirmed.
- Raising reference clock up to 110 MHz, the bin size of 0.28 nsec can be achieved.





The digital part of the mezzanine card has been tested!

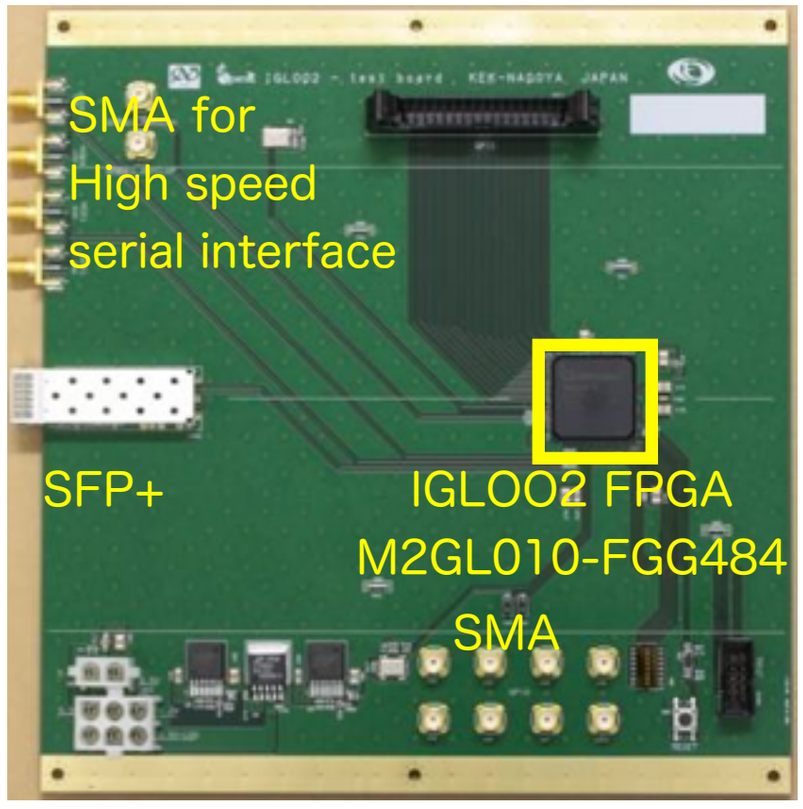
→ Extracting drift-time information from MDT hits is on going.

Radiation tolerant FPGA

- Choosing radiation tolerant FPGA is crucial for the TGC/MDT electronics upgrades
  - SRAM type (e.g. Xilinx-Kintex) is expected to have high radiation tolerance against the total ionization dose (TID), but low radiation tolerance against the single event effect (SEE).
  - Flash memory type (e.g. Microsemi-IGLOO2) is expected to have high radiation tolerance against SEE
- We produced a test board checking radiation tolerance of IGLOO2 FPGA.
- γ irradiation test has been performed and found:
  - Downloading firmware got impossible within 100 Gy.
  - Logics already downloaded seem to survive with a higher dose of 100-200 Gy.

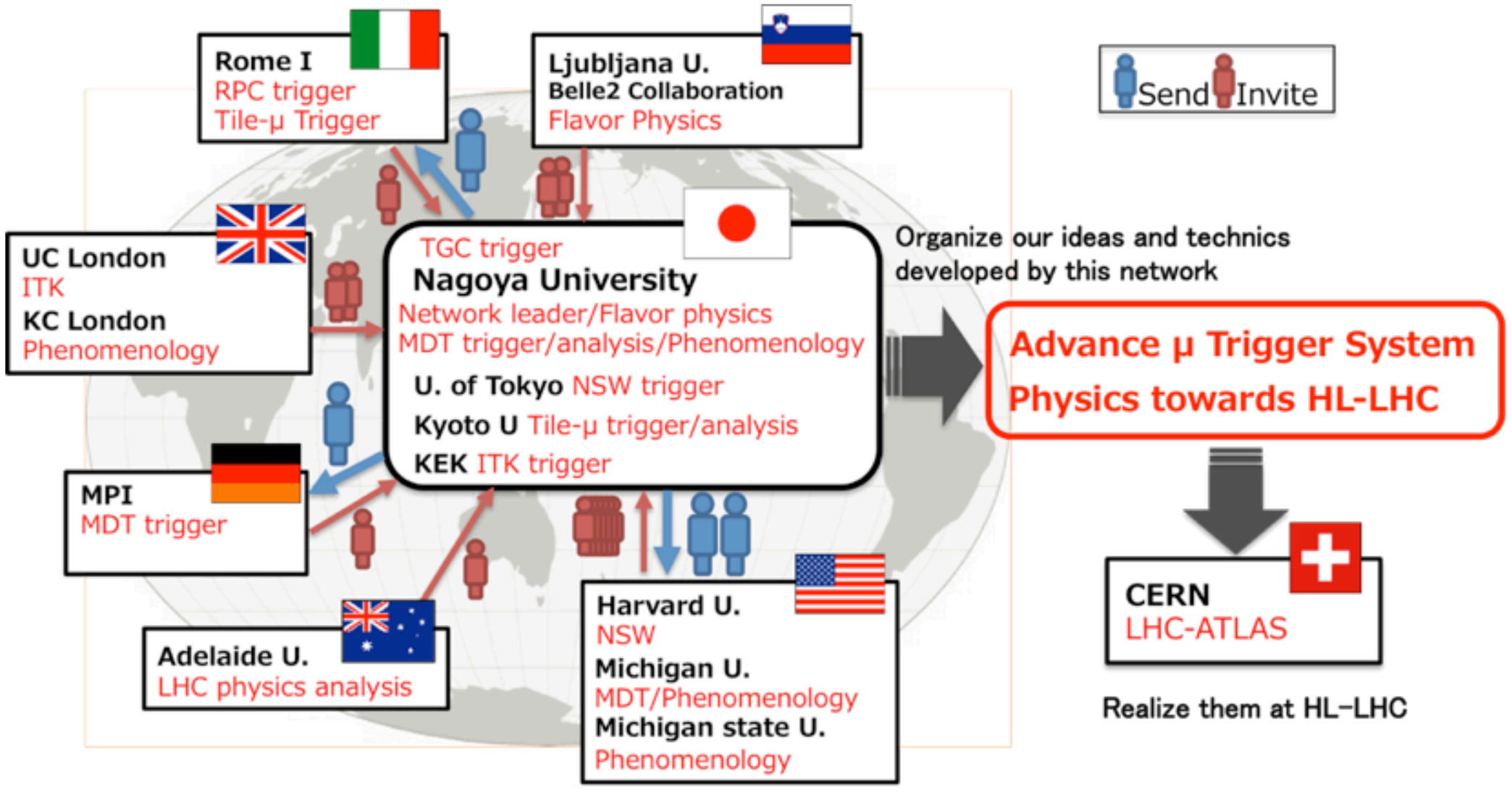
  ➡Depending on the location of the front-end electronics in ATLAS, IGLOO2 FPGA can/cannot be used for HL-LHC.
- Further studies of radiation tolerant FPGA is needed.
  - Rad-tolerance of IGLOO2 FPGA against SEE
  - Rad-tolerance of Kintex FPGA against TID and SEE

Y. Sano



JSPS grant

“Formation of the international network to challenge the discovery of the new particles from the advanced muon trigger development”



I Development of the advanced μ trigger
- I-1 Advanced TGC/RPC trigger
- I-2 MDT trigger
- I-3 Tile-μ trigger
- I-4 Inner μ detector trigger
- I-5 ITK trigger

II Physics towards HL-LHC
- II-a Data analysis using Run2 data
- II-b Flavor physics
- II-c Phenomenology

Conclusion

- To take full advantage of HL-LHC physics program, replacement of the trigger and readout electronics with longer latency and higher rate is essential.
- We devote our large efforts to developing the front-end boards and trigger algorithm for TGC and MDT tracking trigger.
- The functionalities of the front-end boards has been demonstrated using test beam and test pulse.
- The radiation tolerance of FPGA is under consideration.

Young staffs and students from Nagoya are very active in HL-LHC upgrade project !!

Backup

Muon trigger upgrade

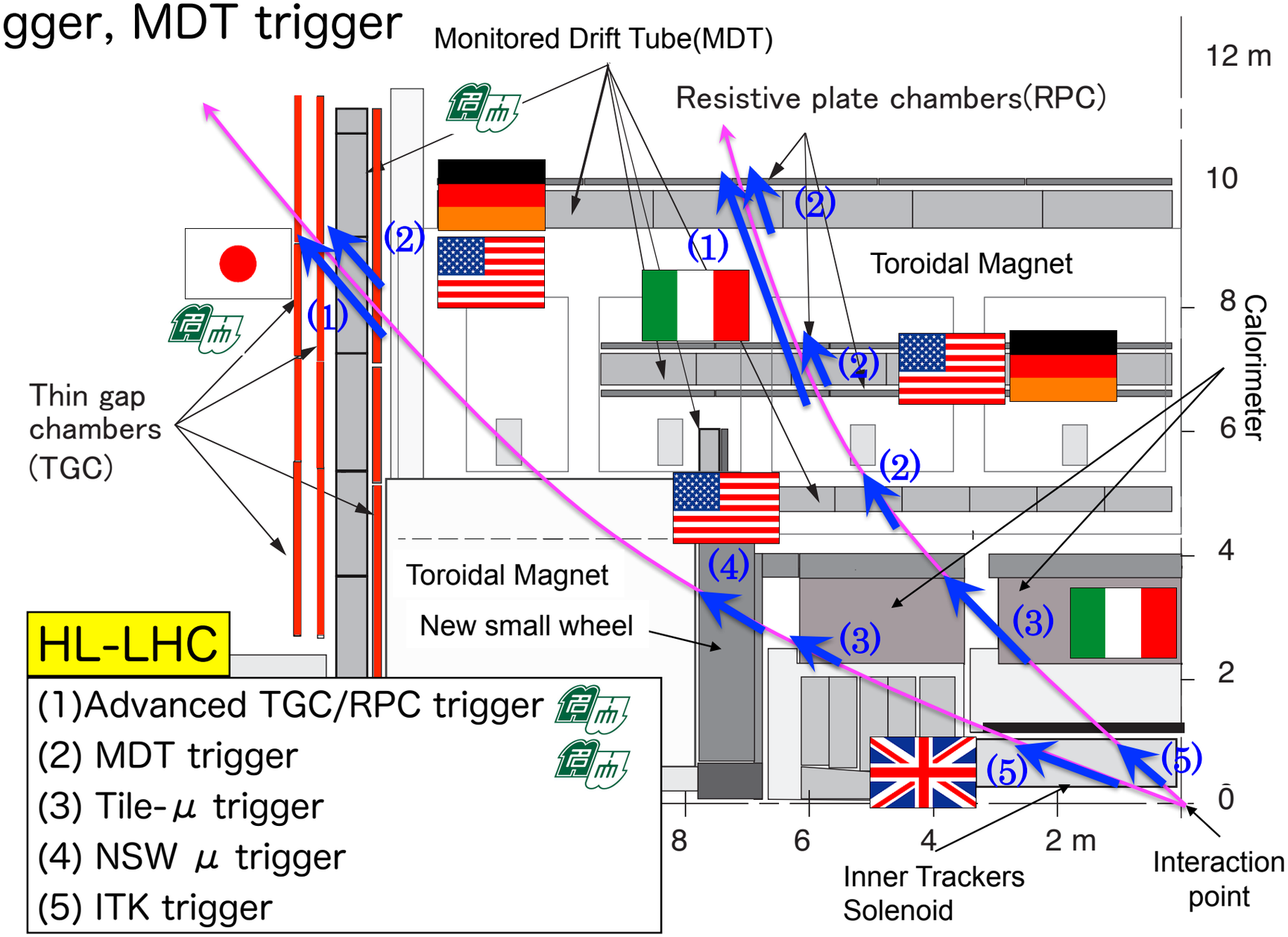
1. Trigger/DAQ scheme upgrade → Replacement of all electronics

   L0 Trigger : latency=6μs, Rate=1MHz

   L1 Trigger : latency=20μs, Rate=400kHz

2. Development of the advanced trigger algorithm

   TGC/RPC track trigger, MDT trigger



Current

(1)TGC/RPC Trigger

HL-LHC

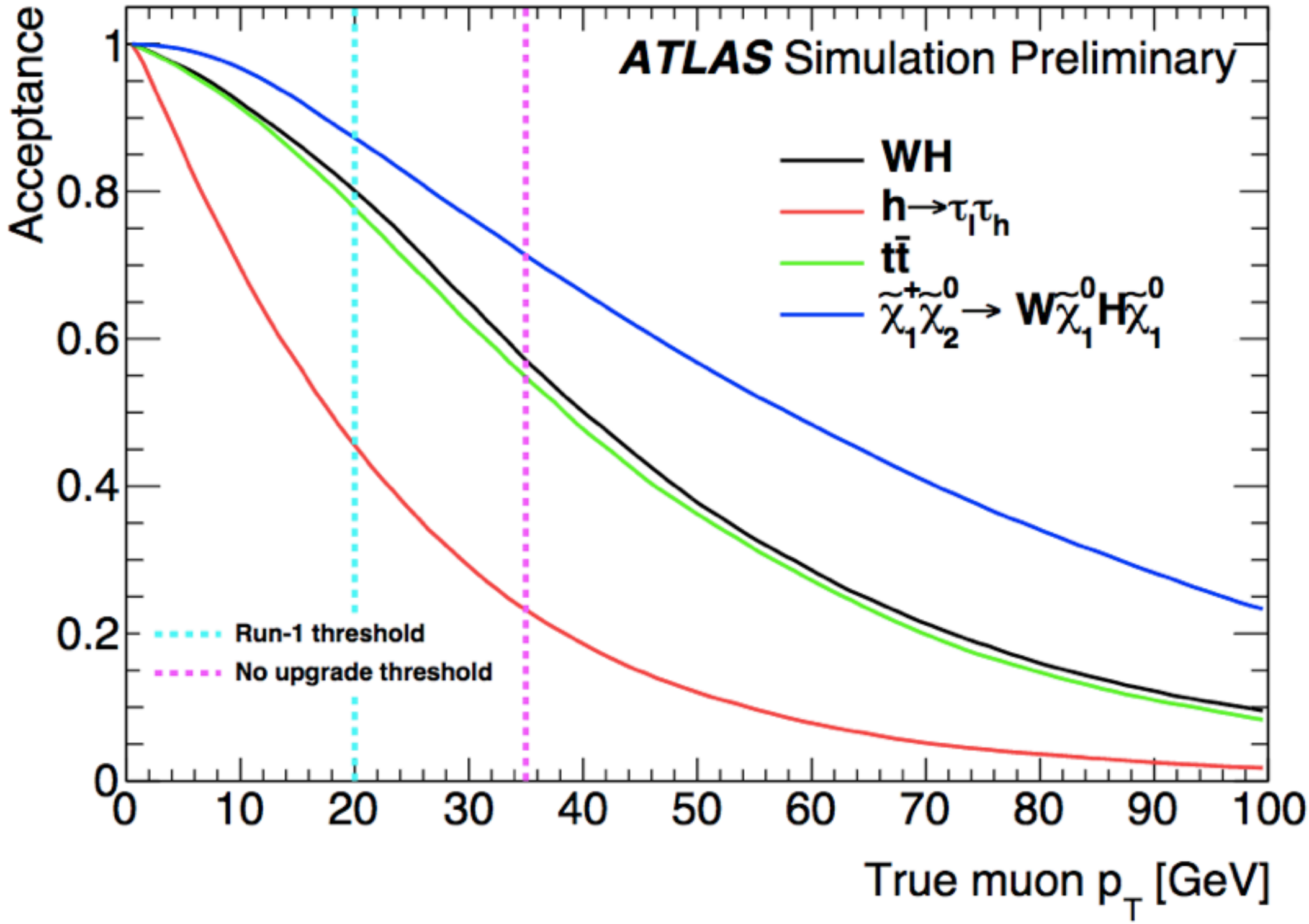
(1)Advanced TGC/RPC trigger

(2) MDT trigger

(3) Tile-μ trigger

(4) NSW μ trigger

(5) ITK trigger


ATLAS Simulation Preliminary
WH
h→τ_lτ_h
tt̄
χ̃₁⁺χ̃₂⁰ → Wχ̃₁⁰Hχ̃₁⁰
Run-1 threshold
No upgrade threshold
Acceptance
True muon p_T [GeV]
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70
80
90
100

FPGA radiation-tolerance study

	Kintex-7 FPGA (Xilinx)	IGLOO2 FPGA (Microsemi)
Configuration memory	SRAM	flash memory
Estimated bit error rate @phase-II	6.5 / 1 h	< 1 / 200 days
TID	~ 10 kGy (65 nm CMOS Vertex-5)	~ 100 Gy (65 nm IGOOL2)

We have produced prototype modules.

We are developing trigger algorithm.