Performance evaluation and electronics development of a new inner-station TGC detector for the ATLAS experiment at HL-LHC

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Introduction

- The HL-LHC is planned to start in 2029. Proton collision data at ATLAS experiment will be obtained up to 4000 fb^{-1}.
  That can improve the sensitivity for searching new particles, including candidates for dark matter.
- To select interesting events from the vast amount of data, upgrades are planned for detector, trigger, and DAQ.
- The TGC detectors used for muon triggers, located inside the magnetic field region, will be changed (Fig. 1).
  - From two layers to three layers
  - To suppress charged particles not directly originating from proton-proton collisions and low momentum muons (Fig. 2).
- The assembly of the first module of the new TGC detector has been completed, and I did a performance evaluation.
  - Measured the noise level and detection efficiency of cosmic muons
  - The DAQ system is based on SoC device

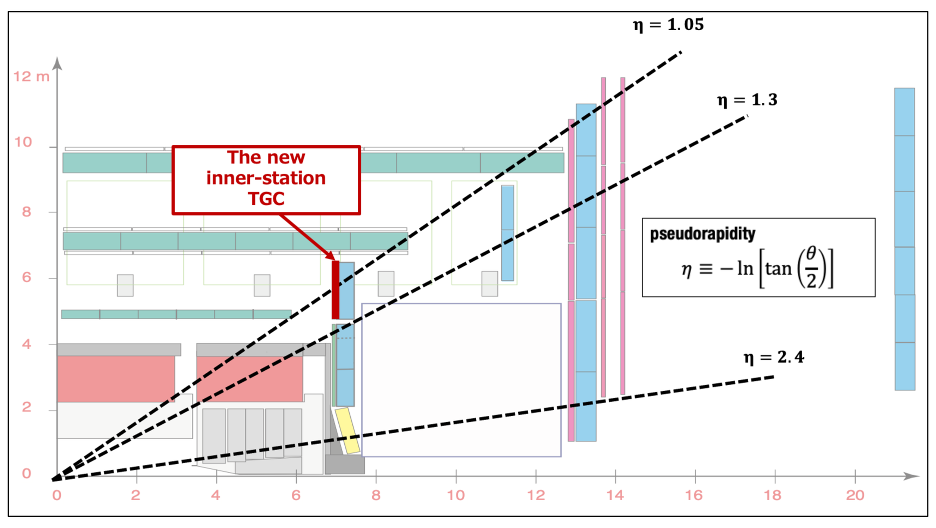

Figure 1: Location of the new inner-station TGC

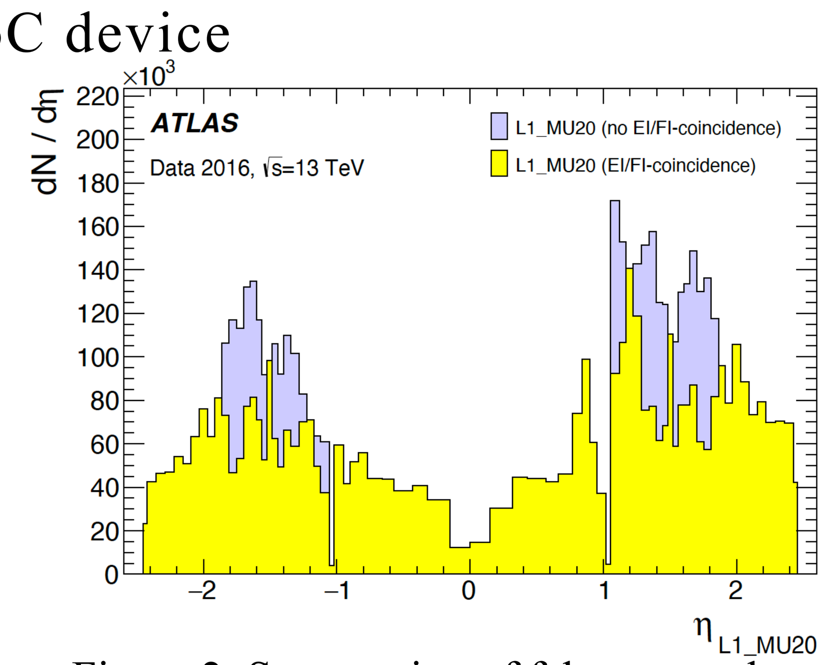

Figure 2: Suppression of fake muons by inner-station TGC detector

TGC detector and DAQ system for Performance evaluation

New inner-station TGC detector

- Three layers structure for both wire and strip (Fig. 3).
- The same thickness as two-layer detector.
- The study of noise level and detection efficiency are key ingredients of the performance evaluation.

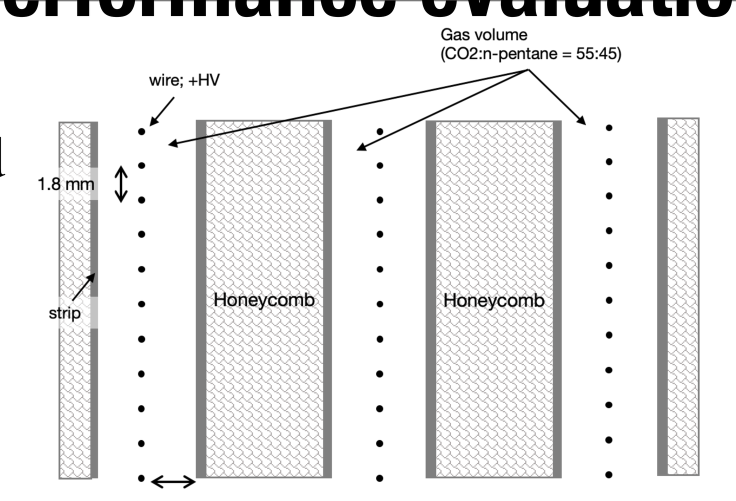

Figure 3: Internal structure of TGC detector

DAQ system

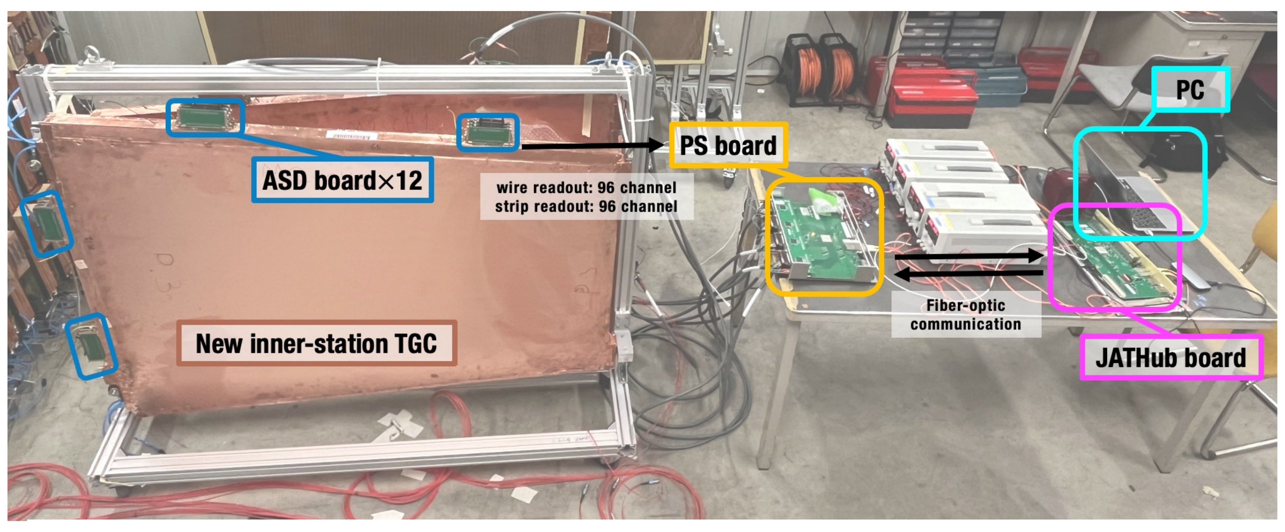

Figure 4: Setup of the experiment

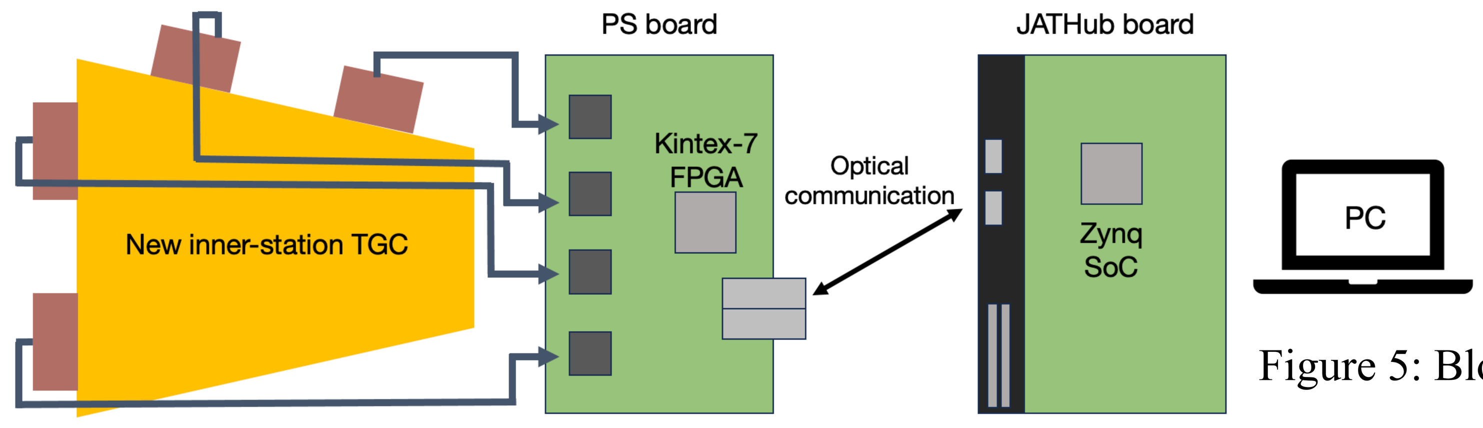

Figure 5: Block diagram of setup

The TGC hits are digitized on the ASD board, synchronized to 40 MHz by the PP ASIC on the PS board, and then sent to the JATHub (Fig. 4). JATHub receives 256-bit hit data from the PS board every 25 ns via optical communication (Fig. 5). It buffers the received data and its associated timing. When the trigger accept signal (L1A) is provided, the data are transferred to a FIFO memory. The data stored in the FIFO memory are read out by the CPU.

Noise evaluation

- **Average noise rate per PP ASIC**
  - Random trigger
  - Accumulated data: 1176500 events
  - Noise rate = Number of hits / 1176500
  - Error bars show standard deviation (variation per channel is visible)
  - Threshold voltage for the comparator of ASD boards
    Vth = 0, 10, 20, 30, 40, 50, 60, 70, 80, 90, 100 mV

Noise Evaluation (continued)

- **Result for Module 1**
  - Noise disappears at Vth ≥ 20 mV for wire
  - Noise disappears at Vth ≥ 90 mV for strip
  - Module 1 can use the normally used Vth=60 mV for wire, while strip requires Vth=90 mV.
- **Result for Module 2 (Fig. 6)**
  - Noise disappears at Vth ≥ 20 mV for wire
  - Noise disappears at Vth ≥ 50 mV for strip
  - Module 2 can use the normally used Vth=60 mV(wire), and 70 mV(strip) for both wire and strip.

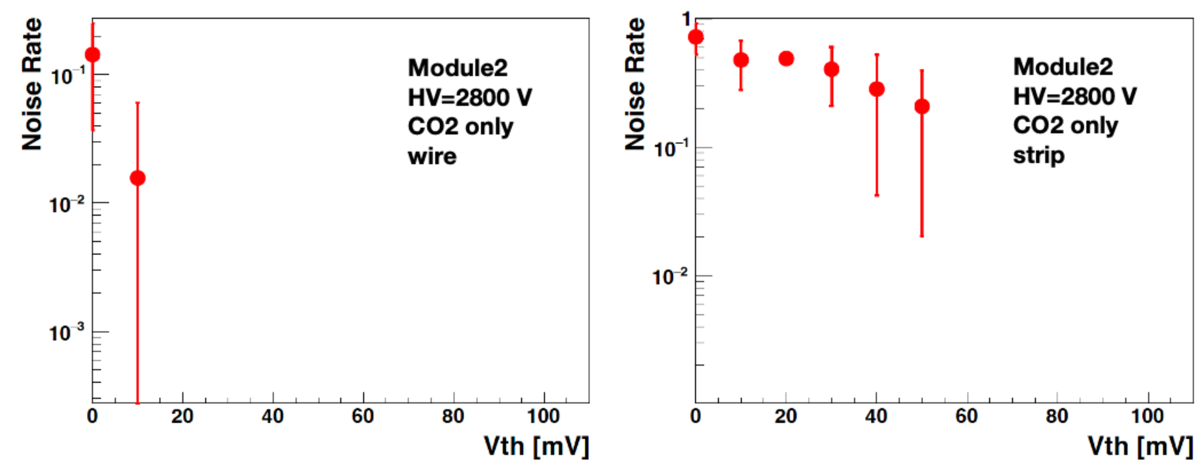

Figure 6: Analysis results of noise evaluation (left: wire, right: strip)

Efficiency evaluation

- Self trigger: hits required for at least two layers (Fig. 7)
- The detection efficiency of the current outer layer TGC detector is 92-93% and the new detector should have comparable efficiency.
- HV=2800 V, threshold voltage=100 mV, CO2 + n-pentane
- Accumulated data: 1,000,000 events

$$\text{Efficiency} = \frac{\text{(Number of hits on all 3 layers of wires, strips)}}{\text{(Number of hits on layer 0 and layer 2 wires and strips)}}$$

- Efficiency for wires: 94.0 ± 0.1%
- Efficiency for strips: 92.2 ± 0.1%
- The measured efficiency is consistent with the expectation; the inefficiency is due to internal support structure.
- The hit distribution on layer 1 (Fig. 8) represents the trapezoidal shape of the detector.

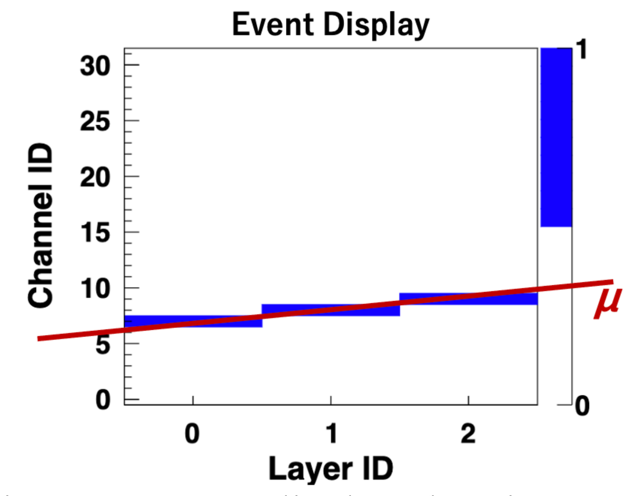

Figure 7: Event display showing muon hits

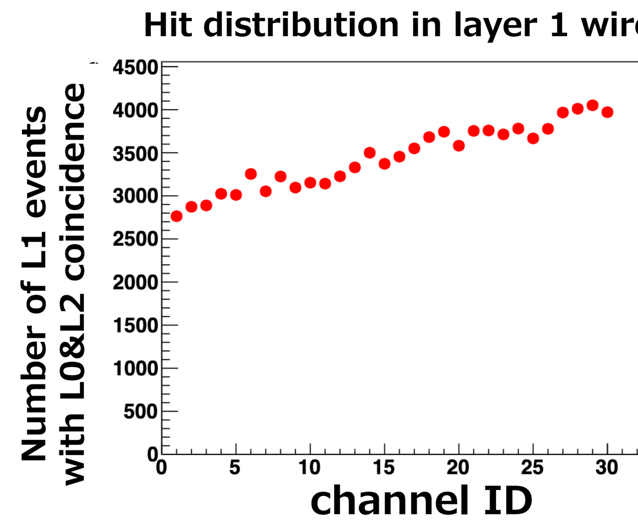

Figure 8: Hit distribution in layer 1 wire when a hit is requested on layer 0 and layer 2 wires

Trigger logic for a new inner-station TGC

- Developed a trigger circuit for the operation (Fig. 9)
- Designed a coincidence circuit with a latency of 25 ns
- All proton-proton crossings occurring every 25 ns are treated exactly the same

3 out of 3 coincidence logic

Position 5 = Layer 1 (1) & Layer 2 (2) & Layer 3 (2)

3 out of 2 coincidence logic

Position 5

= (Layer 1 (1) & Layer 2 (2) & $\overline{\text{Layer 3(2)}}$)

|| (Layer 1 (1) & $\overline{\text{Layer 2(1)}}$ & $\overline{\text{Layer 2(2)}}$ & Layer 3(2))

|| ($\overline{\text{Layer 1(1)}}$ & $\overline{\text{Layer 1(2)}}$ & Layer 2(2) & Layer 3(2))

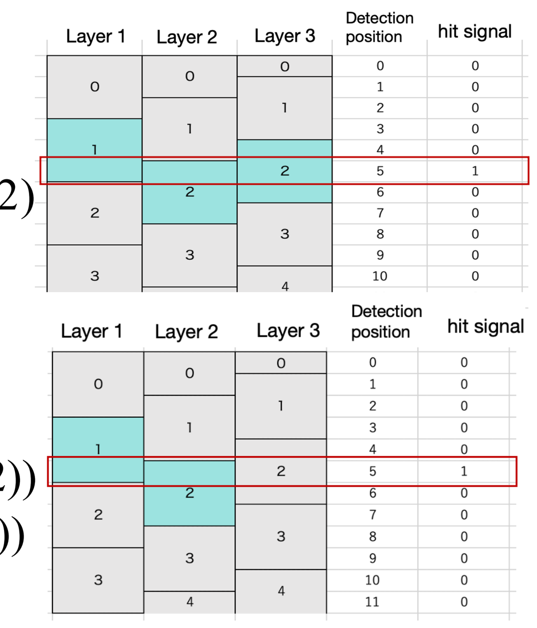

Figure 9: Example of how to take coincidence

Simulation

- The correct output was obtained for 2428 different input patterns without a single bit being wrong.

Summary

- The ATLAS experiment will be upgraded for the HL-LHC to be started in 2029.
- The performance of the new inner-station TGC was evaluated (noise and efficiency) and a coincidence circuit was developed.
- The threshold voltages for eliminating noise were found to be wire:60 mV, strip:70-90 mV.
- The detection efficiency was found to be wire: 94.0 ± 0.1%, strip: 92.2 ± 0.1%.
- The coincidence circuit for the new inner station TGCs was confirmed with logic simulation.

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